

A Design Methodology for Switched-Capacitor DC-DC Converters

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14. ABSTRACT <p>Switched-capacitor (SC) DC-DC power converters are a subset of DC-DC power converters that use a network of switches and capacitors to efficiently convert one voltage to another. Unlike traditional inductor-based DC-DC converters, SC converters do not rely on magnetic energy storage. This fact makes SC converters ideal for integrated implementations, as common integrated inductors are not yet suitable for power electronic applications. While they are only capable of a finite number of conversion ratios, SC converters can support a higher power density compared with traditional converters for a given conversion ratio. Finally, through simple control methods, regulation over many magnitudes of output power is possible while maintaining high efficiency. A complete, detailed methodology for SC converter analysis, optimization and implementation is derived. These methods specify device choices and sizing for each capacitor and switch in the circuit, along with the relative sizing between switches and capacitors. This method is advantageous over previously-developed analysis methods because of its simplicity and the intuition it lends towards the design of SC converters. The strengths and weaknesses of numerous topologies are compared amongst themselves and with magnetics-based converters. These methods are incorporated into a MATLAB tool for converter design. This design methodology is applied to three varied applications for SC converters. First a high-voltage hybrid converter for an autonomous micro air vehicle is described. This converter, weighing less than 150mg, creates a supply of 200V from a single lithium-ion cell (3.7V) to supply the aircraft's actuators. Second, a power-management integrated circuit (IC) is presented for a wireless sensor node. This IC, with a target quiescent current of 1 A supplies the system voltages of the PicoCube wireless sensor node. Finally, the initial design of a high-current-density SC voltage regulator is presented for low-footprint microprocessor applications.</p>		
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A Design Methodology for Switched-Capacitor DC-DC Converters

by

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Abstract

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A complete, detailed methodology for SC converter analysis, optimization and implementation is derived. These methods specify device choices and sizing for each capacitor and switch in the circuit, along with the relative sizing between switches and capacitors. This method is advantageous over previously-developed analysis methods because of its simplicity and the intuition it lends towards the design of SC converters. The strengths and weaknesses of numerous topologies are compared amongst themselves and with magnetics-

based converters. These methods are incorporated into a MATLAB tool for converter design.

This design methodology is applied to three varied applications for SC converters. First, a high-voltage hybrid converter for an autonomous micro air vehicle is described. This converter, weighing less than 150mg, creates a supply of 200V from a single lithium-ion cell (3.7V) to supply the aircraft's actuators. Second, a power-management integrated circuit (IC) is presented for a wireless sensor node. This IC, with a target quiescent current of $1\ \mu A$, supplies the system voltages of the PicoCube wireless sensor node. Finally, the initial design of a high-current-density SC voltage regulator is presented for low-footprint microprocessor applications.

Professor Seth R. Sanders
Dissertation Committee Chair

Contents

Contents	i
List of Figures	v
List of Tables	viii
Acknowledgments	ix
1 Introduction	1
1.1 Switched-Capacitor Converters in Industry and Literature	1
1.2 Switched-Capacitor Converter Structure and Terminology	2
1.3 Pre-existing Switched-Capacitor Converter Analysis	6
1.4 Developments in This Work	7
2 Fundamental Analysis of Switched-Capacitor Converters	10
2.1 Slow-Switching Limit Impedance	11
2.1.1 Extension to Non-Linear Capacitors	16
2.2 Fast-Switching Limit Impedance	18
2.3 Calculating Total Output Impedance	21
2.4 Model Simplification for Two-Phase Converters	24
2.5 Modeling Other Converter Loads	24
2.5.1 Capacitive Loads	25
2.5.2 Current-Source Load	26
2.5.3 Inductive Load	26

3	Optimization of Switched-Capacitor Converters	31
3.1	Device Cost Metrics	32
3.2	Component Sizing	33
3.2.1	Capacitor Sizing	35
3.2.2	Switch Sizing	37
3.2.3	Optimizing Using Other Metrics	38
3.3	System-Level Converter Optimization	41
3.3.1	Converter Loss Components	41
3.3.2	Numerical Optimization	43
4	Comparing Switched-Capacitor Topologies	48
4.1	Converter Performance Metrics	49
4.2	Analysis of SC Topologies	50
4.2.1	Ladder Topology	51
4.2.2	Dickson Charge Pump	55
4.2.3	Fibonacci Topology	56
4.2.4	Series-Parallel Topology	58
4.2.5	Doubler Topology	60
4.3	Comparison of SC Topologies	61
4.3.1	Symmetrical Topologies	64
4.4	Comparison with Magnetics-Based Converters	66
4.4.1	Switch Comparison	67
4.4.2	Reactive Element Comparison	71
4.5	Fundamental Performance Limits	75
4.5.1	SSL Converter Metric Limit	76
4.5.2	FSL Converter Metric Limit	78
5	Regulation of Switched-Capacitor Converters	81
5.1	Output Ripple of Multiphase Converters	83
5.2	Hysteretic Feedback Methods	88
5.3	System Modeling	91
5.4	A Multi-Ratio Converter for Portable Electronics	93
5.4.1	Topology Description	94

5.4.2	Control Method	96
5.4.3	Experimental Results	100
6	High-Voltage Converters for Airborne Robotics	102
6.1	Comparison of Topologies for Lightweight High-Voltage DC-DC Converters	103
6.1.1	Boost Converter	107
6.1.2	Flyback Converter	110
6.1.3	Hybrid Switched-Capacitor Boost Converter	112
6.2	MicroGlider Power Converter	116
7	Switched-Capacitor Converters for Wireless Sensor Nodes	119
7.1	Application and IC Overview	120
7.2	Converter Architecture and Optimization	123
7.3	Gate Drive	126
7.4	Synchronous Rectifier	128
7.4.1	Impedance matching AC energy harvesters with diode rectifiers . . .	132
7.5	Ultra-Low-Power Analog Circuits	134
7.6	System Efficiency	141
8	Switched-Capacitor Converters for Microprocessors	142
8.1	Power Density vs. Scaling	143
8.2	Converter Design	145
8.2.1	Dynamic Voltage Scaling Analysis	147
8.2.2	Cell design	150
8.3	Efficiency Improvements	153
8.3.1	Resonant Gate Drive	154
8.3.2	Drain Charge Recovery	155
8.3.3	Reducing Bottom-Plate Capacitance	158
9	Conclusions	161
A	Network-Theory-Based Analysis for Switched-Capacitor Converters	164
A.1	Summary of Circuit Theory	164
A.2	Modeling Switched-Capacitor Networks	167
A.2.1	Finding the Conversion Ratio and Component Voltages	168

A.2.2	Determining the Charge Multiplier Vector	170
A.3	Criteria for Properly-Posed SC Topologies	176
A.4	Converter Dynamics	180
A.4.1	Preparing the System	181
A.4.2	Single-Phase Dynamics	182
A.4.3	Discrete-Time Model	186
A.4.4	Dynamics Simulation	188
B	MATLAB Package for Switched-Capacitor Converter Design	190
B.1	Core Functions	191
B.2	Visualization Functions	196
B.3	Helper Functions	199
B.4	Example	200
B.5	Code Listings	204
B.5.1	evaluate_loss.m	204
B.5.2	generate_topology.m	207
B.5.3	implement_topology.m	212
B.5.4	optimize_loss.m	215
B.5.5	permute_topologies.m	216
B.5.6	plot_opt_contour.m	217
B.5.7	plot_regulation.m	219
B.5.8	techlib.m	222
	Bibliography	225
	Index	231

List of Figures

1.1	An idealized 3-port SC converter	3
1.2	A 3:1 ladder topology, including networks in (b) phase 1 and (c) phase 2 . .	4
1.3	Idealized 2-port SC converter model	5
2.1	A 3:1 ladder topology	12
2.2	Capacitor charge flow in ladder converter. (a) phase 1 and (b) phase 2 . . .	12
2.3	Energy loss due to capacitor charging	16
2.4	Nonlinear capacitor losses in a three-phase converter	17
2.5	Switch charge flow in ladder converter: (a) phase 1 and (b) phase 2	19
2.6	Trivial SC converter used for dynamic analysis	22
2.7	Capacitor voltage waveform of trivial converter	22
2.8	Output impedance when $R_{SSL} \approx R_{FSL}$ and approximations	27
2.9	2:1 ladder converter: (a) topology (b) waveforms for current and voltage source loads	27
2.10	SC converter with inductive load: a) phase 1 network, b) phase 2 network, c) waveforms	28
2.11	Output impedance of SC converter with inductive load	30
3.1	Example SC converter optimization plot	45
3.2	Example efficiency contour plots of a 3:1 series-parallel converter	46
4.1	Five common switched-capacitor converter topologies in their step-up form	52
4.2	A 2:5 ladder topology	53
4.3	A 2:5 series-parallel topology	59
4.4	Comparison of SSL and FSL converter metrics	63
4.5	Symmetric 2:5 ladder topology	65

4.6	SSL metric improvement with symmetric converters	66
4.7	Traditional magnetics-based converters	67
4.8	FSL metrics for magnetics-based and SC converters	70
4.9	SSL metrics for magnetics-based and SC converters	74
5.1	Efficiency during power backoff; 2:1 converter	83
5.2	Current transfer and output voltage ripple waveforms of a regulated four-phase 2:1 converter	86
5.3	Output voltage ripple of an N -interleaved-phase 2:1 converter	87
5.4	Double-bound hysteresis feedback for the PicoCube application	89
5.5	Lower-bound hysteretic feedback controller	90
5.6	Waveform from lower-bound feedback-based converter	91
5.7	Idealized dynamics model for system modeling	92
5.8	$\{5, 6, 7, 8\}$: 7 ladder topology stage	94
5.9	3:1, 2:1 Dickson topology stage	95
5.10	Predicted efficiency of multi-ratio converter	97
5.11	Controller for the multi-ratio converter	98
5.12	Operation regions for the multi-ratio converter	99
5.13	Output voltage and efficiency of the multi-ratio converter prototype	101
6.1	Three topologies for lightweight, high-voltage DC-DC conversion	104
6.2	Available (a) capacitors by voltage and (b) inductors by current	106
6.3	Hybrid switched-capacitor boost converter	112
6.4	Photos of the MicroGlider and control PCB	117
6.5	Hybrid SC boost converter as appearing on the MicroGlider	117
7.1	Photos and dimensions of the a) PicoCube and the b) electromechanical shaker	120
7.2	Measurement and transmission power	121
7.3	Block diagram of the converter IC	122
7.4	Switch-level diagram of a) 1:2 converter, b) 3:2 converter	123
7.5	Optimization contours of the (a) 1:2 converter and (b) 3:2 converter	125
7.6	Cascode level-shift gate drive for the 1:2 ladder converter	127
7.7	Capacitor-boost gate drive for the 3:2 converter	128
7.8	Shaker (a) design and (b) example input waveform	129

7.9	Synchronous rectifier circuit	130
7.10	Circuits implementing the synchronous rectifier	131
7.11	Available energy via rectification into a fixed voltage source	133
7.12	Diagram of control logic	135
7.13	Schematics of analog references	136
7.14	Low-leakage sample and hold circuit	136
7.15	Photomicrograph of power interface IC	137
7.16	SC Converter output voltage and efficiency, $V_{in} = 1.15V$	138
7.17	Power output and efficiency of synchronous rectifier, $V_B = 1.2V$, $R_S = 2.0k\Omega$, 100 Hz input	139
7.18	Synchronous rectifier waveforms (at 100 Hz)	140
8.1	SC converter performance versus ITRS technology node	145
8.2	Triple-ratio topology and its switch configurations	146
8.3	Efficiency plot of triple-ratio topology in a 32nm process	147
8.4	Approximate ring oscillator performance versus supply voltage	149
8.5	Energy per operation using an SC converter	150
8.6	Non-scaling components of power loss versus cell size	153
8.7	Drain charge recovery using a two-interleaved-phase 2:1 converter	156
8.8	Waveforms of drain charge recovery methods	157
8.9	Parasitic capacitance ratios for body and well capacitances	159
A.1	An example circuit with graph representation	165
A.2	3:1 Ladder topology, including twig designations in each phase	168
A.3	Three configurations of a 2:5 series-parallel topology	177
A.4	An improperly-posed switched-capacitor converter	179
A.5	Simulation of the dynamics of 3:1 ladder converter	189
B.1	Example plots from the MATLAB package	202

List of Tables

3.1	Capacitor optimization summary for two device cost bases (two-phase simplifications)	39
3.2	Switch optimization summary for two device cost methods (two-phase simplifications)	39
4.1	Energy densities of common (a) capacitors and (b) inductors	73
6.1	Mass of common surface-mount components	105
6.2	N-channel MOSFETs in SOT-23 package	105
6.3	Efficiency of single-stage boost converter	109
6.4	Efficiency of flyback converter using custom transformer	111
6.5	Efficiency of hybrid boost converter	114
6.6	Efficiency of ladder converter with 4–10 stages at 10 mW load	116
6.7	Experimental results of the MicroGlider converter	118
7.1	Energy efficiency over sensing period	141
8.1	Process parameters from the ITRS roadmap	144
8.2	TDP and pin counts for three modern Intel microprocessors	144

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Chapter 1

Introduction

Switched-capacitor (SC) DC-DC power converters are a subset of DC-DC power converters, using only switches and capacitors, that can efficiently convert one voltage to another. Since SC converters use no inductors, they are ideal for integrated implementations, as common integrated inductors are not suitable for power electronic applications. SC DC-DC converters also exhibit other advantages (and disadvantages) which will be further examined in this work.

1.1 Switched-Capacitor Converters in Industry and Literature

Switched-capacitor converters have been used in commercial products for many years. These parts have been relatively simple, typically providing fixed-ratio conversions (such as a simple doubling, halving or inverting of the voltage). They have historically been used in integrated circuits to provide the programming voltage for FLASH and other re-programmable memories [66], and to generate the voltages required by the RS232 serial communication standard [30]. Additional discrete-capacitor SC converter ICs provide conversion for LED lighting applications, a promising application of SC converters [31].

Only recently have SC converters come to market which utilize advanced techniques. For example, the TPS60311 chip from TI is a single-cell (0.9 V to 1.8 V) to 3.3V converter for consumer products [58]. It supports regulation through the use of two conversion ratios and by varying switching frequency, allowing for precise regulation for IC applications. Additionally, the chip supports an extremely-low standby power ($2\ \mu\text{A}$), allowing its use in ultra-low-power applications, such as wireless sensor nodes.

The LM3352 chip from National Semiconductor[32] is a 200 mA buck/boost DC-DC converter chip. It employs an external-capacitor design using three flying capacitors which supports multiple conversion ratios and full output regulation. These products push SC converters into the space occupied by regulated inductor-based converters.

Improvements in PCB area utilization can be made by moving the capacitors on-chip. The MAX203E RS232 transceiver IC from Maxim uses internal capacitors to generate a $\pm 10\text{ V}$ supply from a single-polarity 5 V input. However, only a miniscule amount of power is available from this part. This research aims to improve the power density and flexibility of on-chip SC DC-DC power converters.

1.2 Switched-Capacitor Converter Structure and Terminology

A switched-capacitor (SC) DC-DC converter is a power converter which is comprised exclusively of switches and capacitors. In general, an SC converter can have an arbitrary number of ports, as shown in figure 1.1. Each port can be connected to a voltage source, current source, resistive load, or any other type of circuit. A converter can be made of any number of series sub-converters, or *stages*, to expand the conversion ratio range.

Additionally, a single-stage SC converter can implement one or several topologies, where the converter is denoted a *multi-ratio* converter. Each *topology* corresponds to a particular configuration of switches and capacitors which achieves a particular conversion ratio. By changing the way the switches in a converter are clocked, a converter can be configured into multiple topologies. A converter stage may also implement a number of parallel copies of

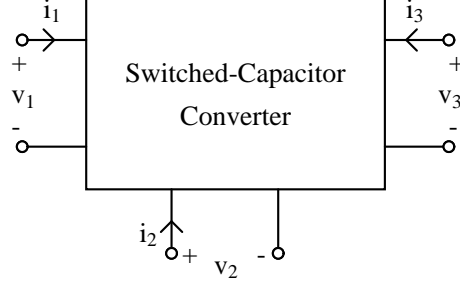


Figure 1.1. An idealized 3-port SC converter

the topology (or set of topologies), each known as an *interleaved phase*. By placing these interleaved phases in parallel, and using equally-spaced interleaved clocking, output ripple frequency will be increased and ripple magnitude will be decreased. Interleaving will be further discussed in section 5.1. If a stage has N interleaved phases, they will be denoted Φ_1 through Φ_N .

Each *topology* consists of a collection of switches and capacitors. Each switch is turned on during one or more phases. Each switching period consists of n non-overlapping subdivisions known as *phases*. These n phases are designated ϕ_1 through ϕ_n . In each clock phase, the switches configure the topology into a network of capacitors and on-state switches (modeled as resistances). By switching through the phases, the topology performs power conversion between its ports.

An example of a ladder-type SC converter topology is shown in figure 1.2. In this topology, the odd-numbered switches are turned on during phase 1 and the even-numbered switches turn during in phase 2. Capacitors C4 and C5 are known as *flying capacitors* since their common-mode voltage moves with respect to ground. Capacitors C1, C2 and C3 have a DC common-mode voltage (i.e. are fixed with respect to ground), and are known as output or bypass capacitors. This two-port converter exhibits a conversion ratio of three-to-one, i.e. the output is one-third of the voltage of the input under no-load conditions. Likewise, the converter multiplies charge by a factor of three.

The requirements placed on an SC topology to be well-posed are discussed in section A.3.

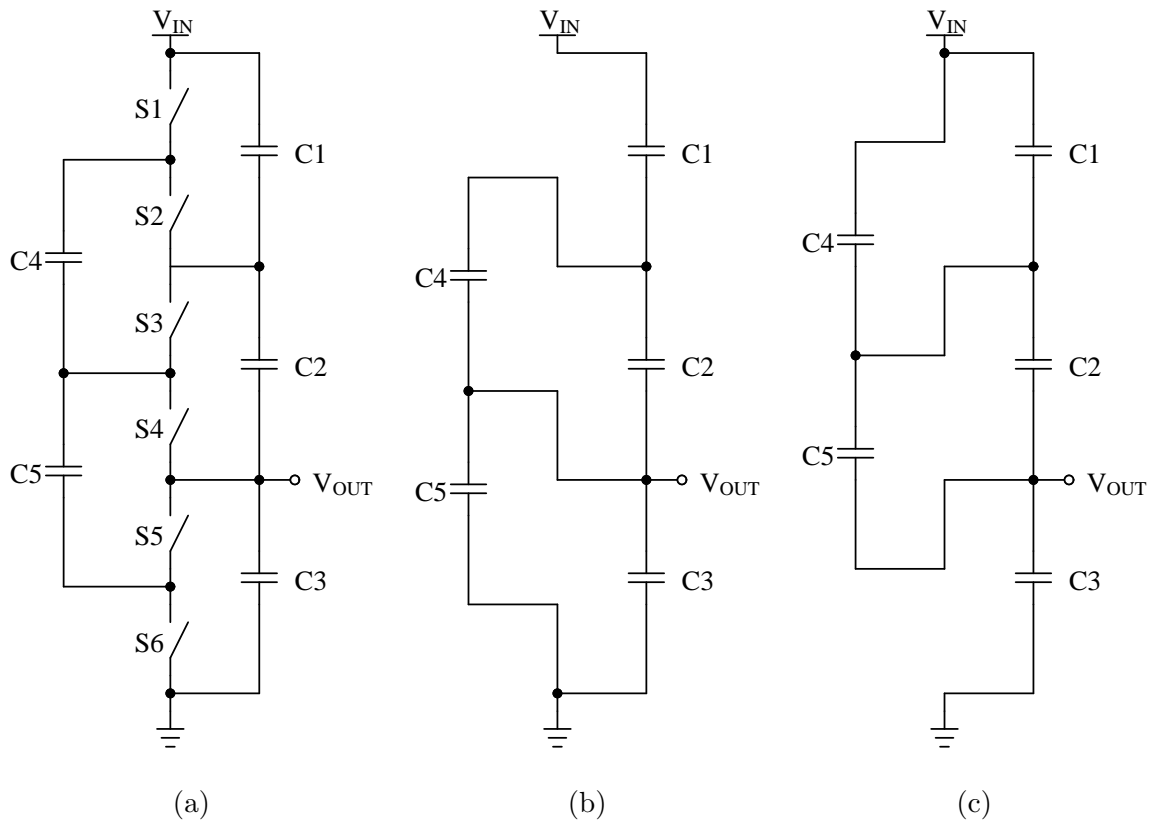


Figure 1.2. A 3:1 ladder topology, including networks in (b) phase 1 and (c) phase 2

First, the no-load case will be examined with idealized components¹. With a DC voltage source applied to one of the converter's ports (designated the *input*), and the remaining ports open-circuited, the clocked converter will operate in a steady-state condition. If the converter is properly posed, as discussed in appendix A.3, a DC voltage should appear at the open-circuited ports, and no steady-state current should flow from the input source. Additionally, each capacitor should support a DC voltage. These criteria ensure that charge is preserved and no shorting events occur.

To transfer charge between the input and output ports of the converter, the converter's capacitors must be charged and discharged, necessitating a voltage drop across the converter. This voltage drop is proportional to output current, and can be represented as an output resistance. An idealized model for a two-port SC converter is shown in figure 1.3, as discussed in references [27, 35]. The model is made up of an ideal transformer with a turns ratio equal to the no-load conversion ratio, and an output resistance R_{OUT} .

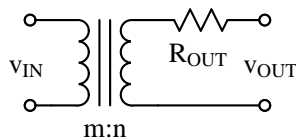


Figure 1.3. Idealized 2-port SC converter model

The low-frequency output impedance R_{OUT} in figure 1.3 sets the maximum converter power, constrained by a minimal efficiency objective, and also determines the open-loop load regulation properties. There are two asymptotic limits to output impedance, the slow and fast switching limits, as related to switching frequency. The *slow-switching limit (SSL)* impedance is calculated assuming that the switches and all other conductive interconnects are ideal, and that the currents flowing between input and output sources and capacitors are impulsive, modeled as charge transfers. The SSL impedance is inversely proportional to switching frequency. The *fast-switching limit (FSL)* occurs when the resistances associated with switches, capacitors and interconnect dominate, and the capacitors act effectively as

¹Ideal components include ideal capacitors and idealized switches with a finite on-state resistance and an infinite off-state resistance.

fixed voltage sources. In the FSL, current flow occurs in a frequency-independent piecewise constant pattern. Computation of the FSL and SSL output impedances will be developed in chapter 2.

Since the model in figure 1.3 perfectly represents the characteristics of an SC converter using ideal capacitors and resistive switches, it can be used to develop a charge conservation constraint. Since the output resistance does not affect the ratio of input to output currents in the model, these two currents are fixed by the transformer turns ratio as:

$$I_{IN} = -\frac{n}{m}I_{OUT} \quad (1.1)$$

Since this charge conservation equality holds independent of load, it can be used for further analysis in later chapters. As this equality also holds on an integral cycle basis, it also can be used to form an input-output constraint on charge flow.

1.3 Pre-existing Switched-Capacitor Converter Analysis

Many papers have attempted analyses of SC converters. One of the early SC papers, [15], introduces and analyzes what is known as the Dickson topology (see section 4.2). However, this analysis assumes a diode-based implementation and only applies for that specific topology family. Numerous additional references [8, 35, 67, 34] follow the same approach and use non-general analysis methods to solve their particular problems. Clearly, a more-unified and general analysis approach is needed.

Maksimovic and Dhar’s groundbreaking work in [27] develops a fundamental model of SC converters and introduces the concept of the slow-switching limit (SSL) impedance. It introduces a network-theoretic method for determining the conversion ratio and SSL output impedance. Since the matrix-based methods are complex, they are not ideal for widespread adoption, and are unnecessary for most analysis of SC converters. Additionally, the analysis method in [27] is not entirely general, and does not address the FSL output impedance besides suggesting its existence. The analysis work in chapter 2 takes this work and extends its simplicity and generality.

1.4 Developments in This Work

The aim of this work is to present a complete analysis and design methodology for SC converters, followed by several descriptions of SC converters being used for various practical applications. Chapter 2 uses the fundamental descriptions from section 1.2 to introduce *charge multipliers* which characterize the charge flows in an SC converter. These charge multipliers are used to find the output impedance of an SC converter.

Chapter 3 uses the simple formulation of the output impedance of an SC converter developed in chapter 2 to develop a method of properly sizing the capacitors and switches. This optimization is based on cost-based metrics where the total device cost (for both capacitors and switches) is limited. This chapter also discusses the system-level design of a converter by choosing the optimal switching frequency and switch area for a given design power.

The merits of different SC topologies are discussed in chapter 4, allowing the selection of the best topology for a given application. The output impedances for numerous topologies, including the ladder, Dickson, series-parallel, Fibonacci and doubler topologies, are compared in both the slow-switching and fast-switching limits. This chapter also compares SC converters to magnetics-based DC-DC converters in terms of both switch and reactive-element utilization. Finally, a fundamental limit on the performance of SC converters is shown in both the SSL and FSL. It is shown that SC converters can achieve a higher power density than magnetics-based converters considering both transistors and reactive elements.

The last of the analysis chapters, chapter 5 discusses the regulation of SC converters. First, the ripple occurring at the output of an SC converter is discussed, including methods of reducing this ripple. Next, simple hysteretic control methods are introduced involving very little circuitry to maintain regulation. A simplified model of SC converters is developed to model and simulate state-based control methods. Finally, a multiple-ratio SC converter for portable electronics is discussed involving both automatic conversion ratio changing and hysteretic feedback to efficiently regulate the output voltage.

Three applications of SC converters are then presented. Chapter 6 compares several DC-DC converters used to drive piezoelectric actuators for airborne robotics. The hybrid boost-switched-capacitor converter used for a two-gram autonomous glider is presented, including design considerations and performance results. This converter produces 200 V from a 3.6V input at a power level of 10mW with a total component mass of 100 mg.

Chapter 7 describes power conditioning and conversion circuitry used in a cubic-centimeter wireless sensor node. A synchronous rectifier efficiently harvests energy from an electromagnetic energy scavenger, charging a small nickel-metal-hydride cell. Two SC converters supply the loads in the sensor at their required voltages. The design and performance of this power management IC are presented. The converter achieves an efficiency of 84% while consuming less than 10 μ W with no load.

This work opens the door towards high-performance, high-power density SC converters. Chapter 8 discusses using SC converters for very high-power applications using entirely-integrated converters. This chapter introduces a multiple-ratio converter which can be integrated on the same die as mainstream microprocessors to supply power to individual cores of a multi-core processor. The power density of SC converters is examined with regard to process scaling. In addition, methods of increasing the efficiency of high-power-density SC converters are introduced. At a power density of 1 W/mm², an efficiency of approximately 80% is predicted.

Finally, this work includes two appendices. Appendix A discusses the network-theoretic analysis of SC converters which can be used to develop CAD tools for the analysis of SC converters. This appendix derives the exact time-based dynamics of an SC converter from the fundamental network matrices for the converter. It also discusses the properties of properly-posed converters.

Appendix B describes a MATLAB package which automates the design process of a SC converter. This package is used several times in this work as a design and visualization tool.

This work aims to present a complete and straightforward design methodology for SC converters. This analysis method will benefit designers greatly in the use of SC converters

for both integrated and non-integrated applications. Three applications using SC converters are also presented, applying the methods developed in this work.

Chapter 2

Fundamental Analysis of Switched-Capacitor Converters

With the model in figure 1.3, the converter provides an ideal dc voltage conversion ratio under no load conditions, and all conversion losses are manifested by voltage drop associated with non-zero load current through the output impedance [27, 35]. The resistive output impedance accounts for capacitor charging and discharging losses and resistive conduction losses. Additional losses due to short-circuit current and parasitic capacitances, in addition to gate-drive losses, can be incorporated into the model. While these parasitic losses are not considered in the analysis in this chapter, they will be incorporated into the system-level design in section 3.3. The aim in this chapter is to provide a general analysis and design framework.

The low-frequency output impedance R_{OUT} in figure 1.3 sets the maximum converter power, constrained by a minimal efficiency objective, and also determines the open-loop load regulation properties. There are two asymptotic limits to output impedance, the slow and fast switching limits, as related to switching frequency [50, 51]. The *slow-switching limit* (SSL) impedance is calculated assuming that the switches and all other conductive interconnects are ideal, and that the currents flowing between input and output sources

and capacitors are impulsive, modeled as charge transfers. The SSL impedance is inversely proportional to switching frequency. The *fast switching limit* (FSL) occurs when the resistances associated with switches, capacitors and interconnect dominate, and the capacitors act effectively as fixed voltage sources. In the FSL, current flow occurs in a frequency-independent piecewise constant pattern. The total output impedance of the converter is a combination of the two impedance components as examined in section 2.3.

The analysis in this chapter is targeted towards a two-port converter, such that R_{OUT} is a scalar. The two-phase model in [48, 51] will be extended here to multi-phase converters, as several of them have been represented in the literature [36]. In this analysis, we will be applying DC voltage sources to both the input (V_{IN}) and the output (V_{OUT}). This allows the determination of the output impedance by calculating the current flowing in the circuit for values of V_{IN} and V_{OUT} . The effect of other loads on efficiency and operation will be discussed in section 2.5.

2.1 Slow-Switching Limit Impedance

For the slow-switching limit (SSL) impedance analysis, the finite resistances of the switches, capacitors, and interconnect are neglected. A set of *charge multiplier vectors* \mathbf{a}^1 through \mathbf{a}^n can be derived for any standard well-posed n -phase SC converter.¹ The charge multiplier vectors correspond to charge flows that occur immediately after the switches are closed to initiate each respective phase of the SC circuit. Each element of a charge multiplier vector corresponds to a specific capacitor or independent voltage source, and represents the charge flow into that component, normalized with respect to the output charge flow. As outlined in [27], the charge multiplier vectors can be uniquely computed using the KCL constraints in each topological phase and the steady-state constraint that the n charge multiplier quantities on each capacitor must sum to zero.

¹If these charge multiplier vectors cannot be uniquely determined, the converter is not well-posed. If a consistent set of capacitor voltages can be found, an excess of DC capacitors (such as decoupling capacitors) prevents a unique vector from being computed.

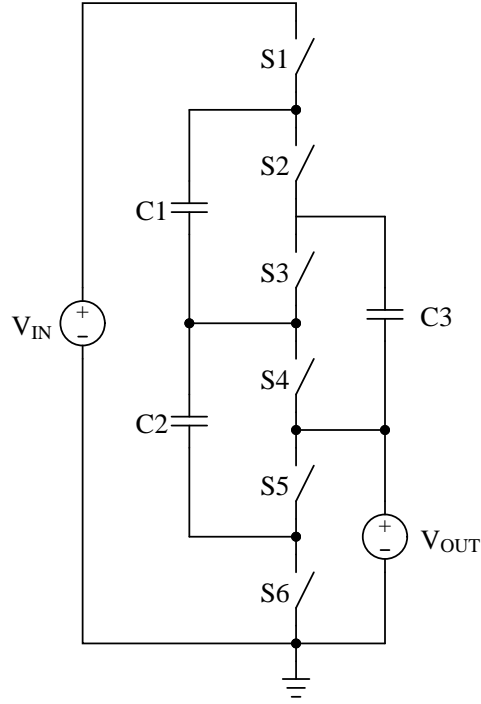


Figure 2.1. A 3:1 ladder topology

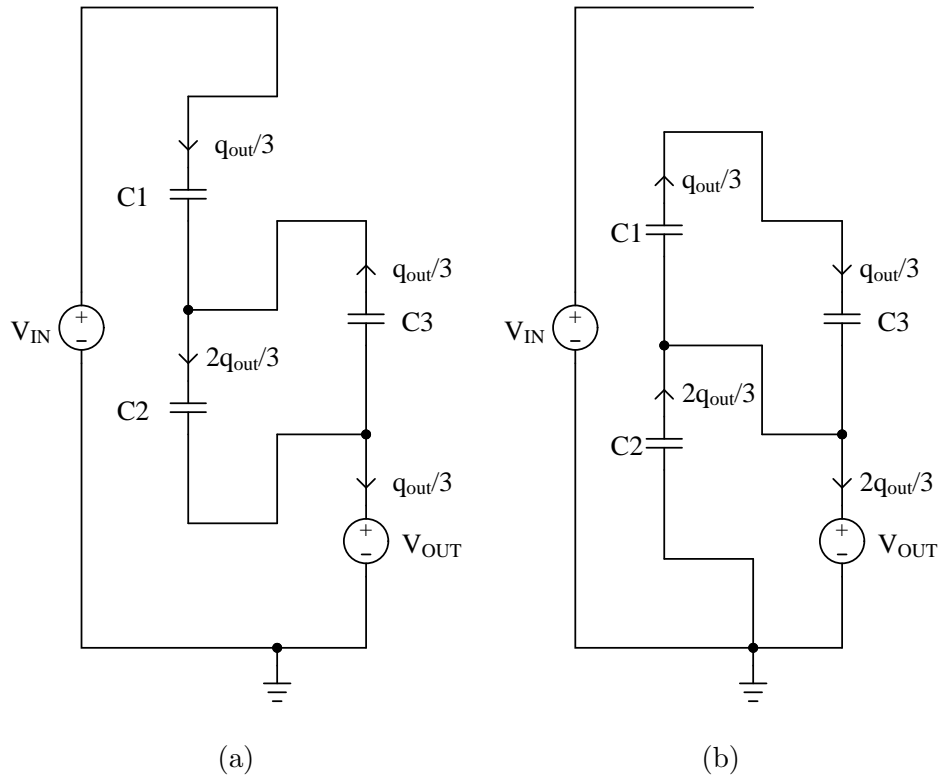


Figure 2.2. Capacitor charge flow in ladder converter. (a) phase 1 and (b) phase 2

The charge multiplier vector \mathbf{a}^1 is defined as:

$$\mathbf{a}^1 = \left[q_{out}^1 \quad q_1^1 \quad \dots \quad q_n^1 \quad q_{in}^1 \right]^\top / q_{out} \quad (2.1)$$

where each component is the ratio of charge transfer in each element during phase 1 of the switching period to the charge delivered to the output during a full period. If charge flows into the positive terminal of the element during phase 1, the corresponding entry in the \mathbf{a}^1 vector is positive. Vectors \mathbf{a}^2 through \mathbf{a}^n are defined analogously for phases 2 through n , respectively. The charge multiplier vector can be partitioned into output, capacitor and input components, respectively:

$$\mathbf{a}^1 = \left[a_{out}^1 \quad \mathbf{a}_c^1 \quad a_{in}^1 \right]^\top \quad (2.2)$$

For the ladder network example of figure 2.1, the charge multiplier vectors can be obtained through network analysis using Kirchoff's Current Law (KCL) [27]. In this example, and in all other examples encountered by the author, the charge multiplier vectors can be obtained by inspection (in figure 2.2). The charge from the input source flows into C1 during phase 1. In phase 2, that charge is transferred into C3. By considering alternating phases, the charge flow in each component can be found:

$$\mathbf{a}^1 = \left[1/3 \quad 1/3 \quad 2/3 \quad -1/3 \quad -1/3 \right]^\top \quad (2.3)$$

$$\mathbf{a}^2 = \left[2/3 \quad -1/3 \quad -2/3 \quad 1/3 \quad 0 \right]^\top \quad (2.4)$$

In each of these charge multiplier vectors, the first component corresponds to the output charge flow, thus these two components must sum to one. The last component of each charge multiplier vector corresponds to the charge flow into the input source, and is non-zero during only phase 1 in this example.

The charge multiplier vectors, the capacitor characteristics, and the switching frequency are the only data needed to determine the output impedance under the asymptotic SSL condition. The calculation, developed here, is based on Tellegen's Theorem [13] which states that for any network, any vector of branch voltages that satisfies KVL is orthogonal

to any vector of branch currents (or equivalently charge flows) that satisfies KCL. This theorem is applied in each of the n phases (or networks) for a n -phase switched capacitor converter operating in periodic steady state, where the input is short-circuited and the output is connected to an independent dc voltage source. The charge flow per period (or average current flow) into the single independent source then defines the output impedance.

Application of Tellegen's theorem to the switched capacitor converter, in each of its n phases (or networks), yields $\mathbf{a}^j \cdot \mathbf{v}^j = 0$, where \mathbf{v}^j is the respective steady state network voltage vectors in phase j . Additively combining these applications of Tellegen's theorem, and noting that the input voltage source has value zero, yields

$$v_{out} \sum_{j=1}^n a_{out}^j + \sum_{i \in caps} \sum_{j=1}^n (a_{c,i}^j v_{c,i}^j) = 0 \quad (2.5)$$

where the first term corresponds to the constant output voltage source and the terms under the summation correspond to the capacitor branches. Recall that $a_{out}^1 + \dots + a_{out}^j = 1$ (as each a_{out}^j is normalized to q_{out}) and that $a_{c,i}^1 + \dots + a_{c,i}^j = 0$ for each capacitor branch, due to charge conservation in periodic steady-state. By defining $\Delta v_{c,i}^j = v_{c,i}^j - v_{c,i}^1$, substituting $\Delta v_{c,i}^j$ into (2.5) yields:

$$v_{out} + \sum_{i \in caps} \left(v_{c,i}^1 \sum_{j=1}^n a_{c,i}^j + \sum_{j=1}^n a_{c,i}^j \Delta v_{c,i}^j \right) = 0 \quad (2.6)$$

$$v_{out} + \sum_{i \in caps} \sum_{j=1}^n a_{c,i}^j \Delta v_{c,i}^j = 0 \quad (2.7)$$

as $a_{c,i}^1 + \dots + a_{c,i}^n = 0$.

It is of direct interest here that none of the capacitor voltages need to be explicitly calculated for this analysis. Rather, $\Delta v_{c,i}^j$ can be computed from the charge flows. In each sub-period, the charge on each capacitor increases proportional to its charge multiplier:

$$v_{c,i}^j - v_{c,i}^{j-1} = \frac{a_{c,i}^j}{C_i} q_{out} \quad (2.8)$$

where C_i is the capacitance value of the i^{th} capacitor, assuming linear capacitors. Thus, $\Delta v_{c,i}^j$ can thus be written as:

$$\Delta v_{c,i}^j = \sum_{k=2}^j a_{c,i}^k \frac{q_{out}}{C_i}. \quad (2.9)$$

Additionally, since the capacitor voltages are cyclic in steady-state, $\Delta v_{c,i}^j$ can also be expressed as:

$$\Delta v_{c,i}^j = - \left(\sum_{k=j+1}^n a_{c,i}^k + a_{c,i}^1 \right) \frac{q_{out}}{C_i}. \quad (2.10)$$

Averaging the two expressions yields:

$$\Delta v_{c,i}^j = \left(-a_{c,i}^1 + \sum_{k=2}^j a_{c,i}^k - \sum_{k=j+1}^n a_{c,i}^k \right) \frac{q_{out}}{2C_i}. \quad (2.11)$$

Substituting (2.11) into (2.7), an expanded equation is generated:

$$\begin{aligned} v_{out} + \sum_{i \in caps} \frac{q_{out}}{2C_i} \left[a_{c,i}^2 (-a_{c,i}^1 + a_{c,i}^2 - a_{c,i}^3 - a_{c,i}^4 - \dots - a_{c,i}^n) + \right. \\ \left. a_{c,i}^3 (-a_{c,i}^1 + a_{c,i}^2 + a_{c,i}^3 - a_{c,i}^4 - \dots - a_{c,i}^n) + \right. \\ \dots \\ \left. a_{c,i}^n (-a_{c,i}^1 + a_{c,i}^2 + a_{c,i}^3 + a_{c,i}^4 + \dots + a_{c,i}^n) \right] = 0. \end{aligned} \quad (2.12)$$

Simplifying (2.12) by expanding and combining like terms yields:

$$v_{out} + \sum_{i \in caps} \frac{q_{out}}{2C_i} \left[-a_{c,i}^1 (a_{c,i}^2 + \dots + a_{c,i}^n) + (a_{c,i}^2)^2 + \dots + (a_{c,i}^n)^2 \right] = 0. \quad (2.13)$$

Realizing that $a_{c,i}^1 = -(a_{c,i}^2 + \dots + a_{c,i}^n)$ allows (2.13) to be further simplified:

$$v_{out} + \sum_{i \in caps} \frac{q_{out}}{2C_i} \sum_{j=1}^n (a_{c,i}^j)^2 = 0. \quad (2.14)$$

Dividing (2.14) by the output current (which can be represented as the product of switching frequency and the periodic output charge) directly yields the average output impedance for the slow-switching asymptotic limit:

$$R_{SSL} = -\frac{v_{out}}{i_{out}} = \sum_{i \in caps} \sum_{j=1}^n \frac{(a_{c,i}^j)^2}{2C_i f_{sw}}. \quad (2.15)$$

This powerful result yields a simple calculation of this asymptotic output impedance and some intuition into the operation of SC converters. The output impedance directly models the losses in the circuit due to capacitor charging and discharging. This impedance can be determined by simply examining the charge flow in the converter without simulation or complicated network analysis.

2.1.1 Extension to Non-Linear Capacitors

The converter's loss in terms of the series output impedance R_{SSL} can be expressed in terms of capacitor loss. A specific capacitor's loss can be related to its voltage swing during a period. While section 2.1 calculated the output impedance of a converter for linear capacitors, the method can be extended to consider non-linear capacitors. This section considers the use of non-linear lossless capacitors in a two-phase converter. During switching phase 1, the i -th capacitor is charged (or discharged) from voltage v_i^2 to v_i^1 . Analogously, during phase 2, the capacitor is then charged from voltage v_i^1 to v_i^2 . Since the charging occurs to completion for operation in the SSL, the energy lost during each transition can be given by the integral:

$$E_{c,i}^1 = \int_{Q_C(v_i^2)}^{Q_C(v_i^1)} v_i^1 - Q_C^{-1}(q) dq \quad (2.16)$$

for the phase 1 transition, where $Q_C(v)$ is the capacitor's nonlinear charge-voltage characteristic, presumed to be invertible. A similar expression exists for the phase 2 transition. These two losses correspond to the two indicated regions in figure 2.3.

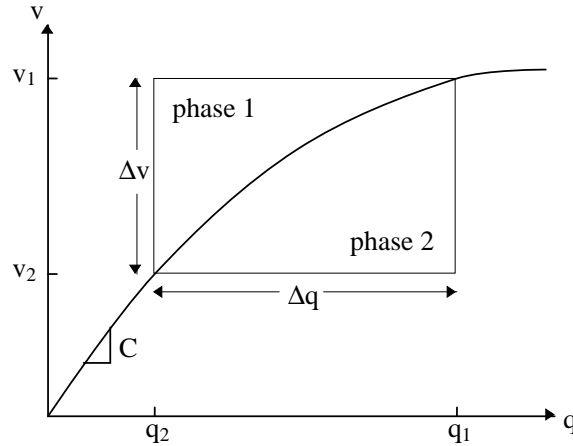


Figure 2.3. Energy loss due to capacitor charging

In the two-phase case, since the total energy lost per period is simply equal to the area of the rectangle, the loss is equivalent to that of a linear capacitor:

$$E_{loss,i} = (v_i^1 - v_i^2) (Q_C(v_i^1) - Q_C(v_i^2)) = C_{eq}(v_i^1 - v_i^2)^2 \quad (2.17)$$

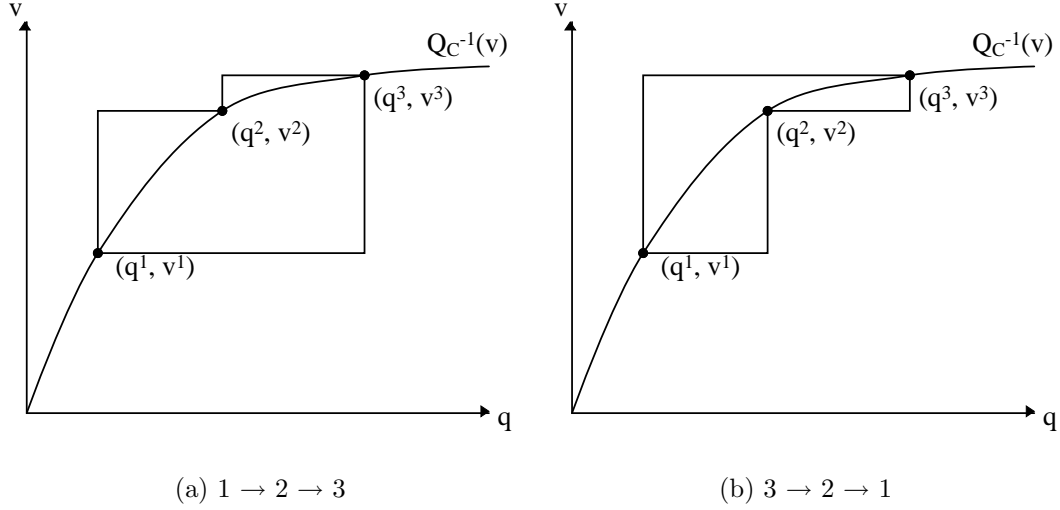


Figure 2.4. Nonlinear capacitor losses in a three-phase converter

where C_{eq} is the linearized capacitance of the capacitor on the chord from v_i^1 to v_i^2 .

The product $a_{c,i}\Delta v_{c,i}$ in (2.7), multiplied by the output charge, represents the energy loss by charging and discharging capacitor i in each cycle. Since this term matches the expression in (2.17) for energy loss, the linearized capacitance C_{eq} can be directly substituted into the output impedance equation (2.15) to find the SSL output impedance of an SC converter with nonlinear capacitors. This expression demonstrates that the sum of the energy lost through the capacitors is equal to the calculated loss associated with the output impedance for a given load.

The effect of nonlinear capacitors in multiphase converters is significantly more complex as the loss region, such as the one in figure 2.4a, is no longer a rectangle. The integrated loss in (2.16) must be used to determine the charging loss of each capacitor in each of the j clock phases. While the exact SSL loss of a multiphase converter using nonlinear capacitors will not be derived, some of the properties of such a converter will be examined.

Consider a three-phase converter using a highly nonlinear capacitor with characteristics shown in figure 2.4a. The three operating points, given by charge-voltage pairs (q^1, v^1) , (q^2, v^2) and (q^3, v^3) are also shown. This converter can either switch from state 1 to state 2 to state 3, and then back to state 1, or in the opposite direction. If linear capacitors are

used, these two methods would yield identical SSL impedances, as the sign of the charge multiplier does not effect the SSL impedance in (2.15). However, in the nonlinear case, the area of the loss region in figure 2.4b is smaller than the loss region in figure 2.4a. Thus, switching from state 3 to state 2 to state 1 and repeating yields lower SSL loss and a lower SSL output impedance. This phenomenon may be used by a designer to improve the performance of a multiphase SC converter if nonlinear capacitors are used.

2.2 Fast-Switching Limit Impedance

The other asymptotic limit, the fast switching limit (FSL), is characterized by constant current flows between capacitors. The switch on-state impedances and other resistances are sufficiently large such that during each phase, the capacitors do not approach equilibrium. In the asymptotic limit, the capacitor voltages are modeled as constant. The circuit loss is related only to conduction loss in resistive elements. The concept of the FSL impedance is introduced informally in reference [35].

The duty cycle of the converter is important when considering the FSL impedance since currents flow during the entirety of each phase. While previous analyses assumed a 50% duty cycle [48, 51], this work will use duty cycle as an input to the model. To keep the analysis general, a duty cycle of D_j will be used for phase j for a converter with n phases. Additionally, only the on-state switch resistance is considered; other parasitic resistance (e.g. capacitor equivalent series resistance (ESR)) can be similarly incorporated into the model if desired.

The $a_{r,i}^j$ charge multipliers are defined as the charge flow through switch i during phase j . Even in the FSL, the charge flows must follow the same pattern as in the SSL, constrained by $\mathbf{a}_{\mathbf{c}}^j$. For each phase, the $a_{r,i}^j$ values for the on-state switches can be determined as a linear combination (typically by inspection) of the capacitor charge multipliers $\mathbf{a}_{\mathbf{c}}^j$. The $a_{r,i}^j$ values for switches that are off are zero. The values of $a_{r,i}^j$ are independent of duty cycle in steady-state as they simply represent the charge flow through the switches that ensure

charge conservation on the circuit's capacitors. The $a_{r,i}^j$ values for the switches in the ladder converter in figure 2.1 can be determined directly. The charge flows in the switches during both phases are shown in figure 2.5, resulting in \mathbf{a}_r^1 and \mathbf{a}_r^2 vectors of:

$$\mathbf{a}_r^1 = \begin{bmatrix} 1/3 & 0 & 1/3 & 0 & -2/3 & 0 \end{bmatrix}^\top \quad (2.18)$$

$$\mathbf{a}_r^2 = \begin{bmatrix} 0 & 1/3 & 0 & 1/3 & 0 & -2/3 \end{bmatrix}^\top \quad (2.19)$$

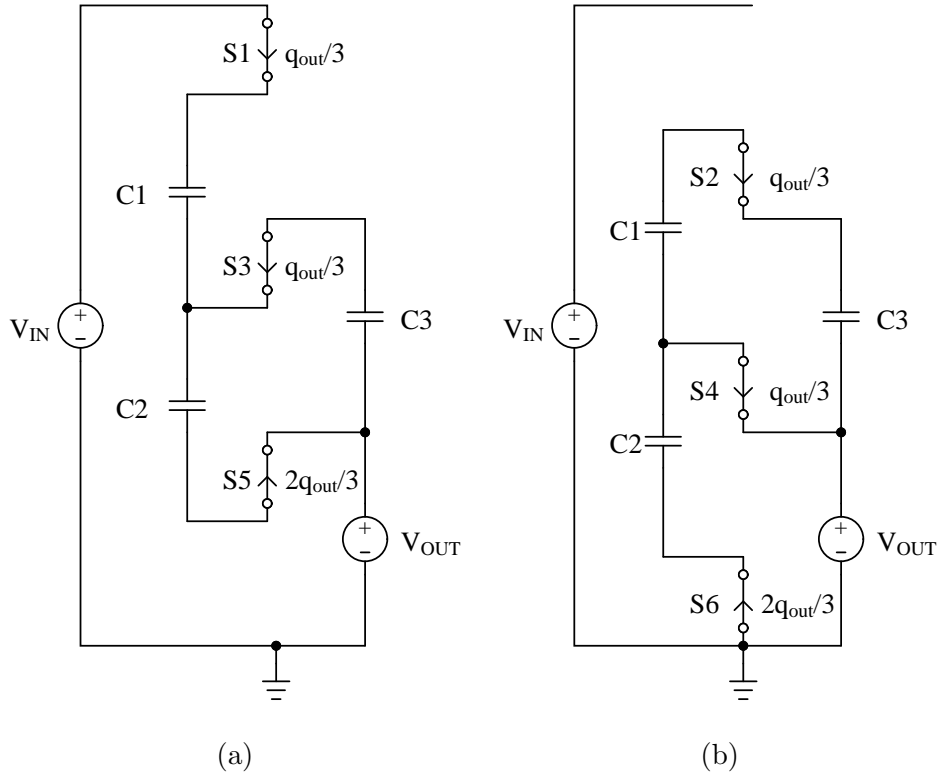


Figure 2.5. Switch charge flow in ladder converter: (a) phase 1 and (b) phase 2

For positive power flow (i.e. from the input to output source), the sign of each component of the \mathbf{a}_r^j vector indicates the direction of current flow with respect to the blocking voltage of a switch during phase j . A positive quantity indicates the switch conducts positive current while on and blocks positive voltage while off. This switch must be implemented using an active transistor. A negative quantity indicates the switch conducts negative current and blocks positive voltage and is suitable for diode implementation (if negative or zero

for all phases, and if the forward voltage drop is tolerable). For power flow in the opposite direction, the switch types reverse.²

In the FSL, the current through the on-state switches is assumed to be constant. Given the charge flow vector, the current in each switch during each phase is easily determined:

$$i_{r,i}^j = \frac{1}{D_j} q_{r,i} f_{sw} \quad (2.20)$$

where $q_{r,i}^j$ is the charge flow through switch i during period j occupying a ratio D_j of the total switching period. Substituting $q_{r,i} = a_{r,i} q_{out}$ and $q_{out} = i_{out} / f_{sw}$ into (2.20) yields:

$$i_{r,i}^j = \frac{a_{r,i}}{D_j} i_{out} \quad (2.21)$$

The current through the switches is only dependent on the \mathbf{a}_r^j vectors, which is obtainable by inspection, and the duration of each period. The network voltages never need to be found in this analysis, simplifying computation significantly.

The average power loss due to each individual switch is equal to the instantaneous on-state power loss multiplied by its duty cycle. Since the total loss of the SC converter in the FSL is just the sum of the switch losses, the total circuit loss is given by:

$$P_{FSL} = \sum_{i \in \text{switches}} \sum_{j=1}^n \frac{R_i}{D_j} \left(2a_{r,i}^j i_{out} \right)^2 \quad (2.22)$$

where R_i is the on-state resistance of switch i .

Since the input and output charge flow in the SC converter is constrained by the conversion ratio n , all the power loss in an ideal SC converter (as analyzed here) is modeled by the output voltage drop. Thus the output impedance can be determined by equating the actual power loss of the circuit with the apparent power loss due to the output impedance. Since this power loss is proportional to the square of the output current, the FSL output impedance can be obtained by inspection:

$$R_{FSL} = \sum_{i \in \text{switches}} \sum_{j=1}^n \frac{R_i}{D_j} (a_{r,i}^j)^2. \quad (2.23)$$

² For multiphase converters, or converters that can be configured to implement several topologies, a particular switch may block bilateral voltage and/or conduct bilateral current, and must be implemented accordingly.

If the total switching period is split into n equal periods, the FSL output impedance can be simplified to:

$$R_{FSL} = n \sum_{i \in \text{switches}} \sum_{j=1}^n R_i (a_{r,i}^j)^2. \quad (2.24)$$

Analogously to the SSL output impedance in (2.15), the FSL output impedance is given simply in terms of component parameters and the switch charge multiplier coefficients of each switch. The power loss due to these conduction losses is equal to the equivalent power loss through the output impedance. These two simple forms of the output impedance (given in (2.15) for the SSL and (2.23) for the FSL) can be used to provide strong guidance for the design of switched-capacitor power converters.

2.3 Calculating Total Output Impedance

The total output impedance of a SC converter is made up of the slow-switching limit (SSL) impedance and fast-switching limit (FSL) impedance, derived in sections 2.1 and 2.2, respectively. However, these components do not directly add to form the total output impedance, as they are derived assuming different operating conditions. When the SSL and FSL impedances are nearly equal, the converter is operating in neither the SSL or FSL, so the assumptions made for each of the two impedance calculations are not valid.

In the operating region between the SSL and FSL, the dynamics of the SC converter play a large roll in determining the impedance. In each phase, the network of on-state switches (modeled as resistors) and capacitors may create very complex settling dynamics for many-element topologies. Since the derivation of the general combined output impedance is impractical, a simple example will be evaluated, and the results will be applied to an approximation of total output impedance. The dynamics of an arbitrary SC converter are developed in section A.4.

In this example, the trivial SC converter, shown in figure 2.6, will be used to examine the output impedance between the slow and fast switching limits. The two switches (each with on-state resistance R) and single capacitor (with capacitance C) guarantee a single

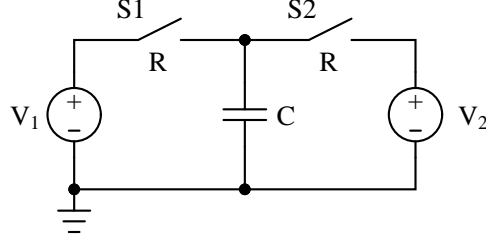


Figure 2.6. Trivial SC converter used for dynamic analysis

settling time constant ($\tau = RC$). Given a switching period T close to the time constant, the converter will be operating in neither the SSL or FSL, so the capacitor voltage will exhibit a waveform like the one shown in figure 2.7.

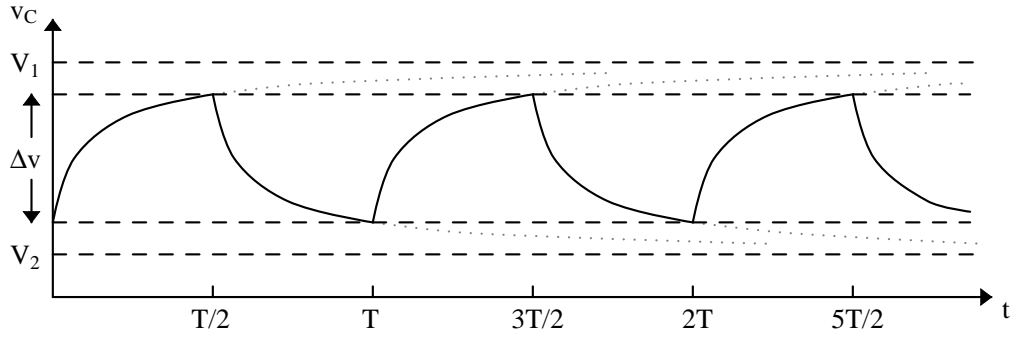


Figure 2.7. Capacitor voltage waveform of trivial converter

The ripple voltage on the capacitor is directly proportional to the charge transfer of the circuit, so the ripple amplitude will be found first. Since the circuit is symmetric and is operating at a 50% duty cycle, the waveform will be symmetric about the mean of V_1 and V_2 . The ripple height can be expressed as a decaying exponential:

$$\Delta v = \left(\Delta v + \frac{V_1 - V_2 - \Delta v}{2} \right) \left(1 - e^{-T/2RC} \right) \quad (2.25)$$

Solving for Δv yields:

$$\Delta v \left(2 - \left(1 - e^{-T/2RC} \right) \right) = (V_1 - V_2) \left(1 - e^{-T/2RC} \right) \quad (2.26)$$

$$\Delta v = (V_1 - V_2) \frac{1 - e^{-T/2RC}}{1 + e^{-T/2RC}} \quad (2.27)$$

Since the charge transferred between sources V_1 and V_2 is proportional to the ripple voltage by $q_{out} = C\Delta v$, the time-averaged current flowing in the circuit is given by:

$$i_{out} = \frac{Cf_{sw} (1 - e^{-T/2RC})}{1 + e^{-T/2RC}} (V_1 - V_2). \quad (2.28)$$

Finally, the output impedance is given by the ratio of output voltage to current, and by substituting $1/f_{sw}$ for the switching period T :

$$R_{OUT} = \frac{1 + e^{-1/2RCf_{sw}}}{Cf_{sw} (1 - e^{-1/2RCf_{sw}})}. \quad (2.29)$$

This form of the output impedance clearly shows the output impedance is not a simple sum between the SSL and FSL output impedance components. Additionally, for networks with more than one mode (or time constant), this expression would become prohibitively complex. The SSL and FSL impedances can be determined by taking the limit of (2.29) as f_{sw} approaches zero and infinity, respectively:

$$R_{SSL} = \lim_{f_{sw} \rightarrow 0} R_{OUT} = \lim_{f_{sw} \rightarrow \infty} \frac{1 + e^{-1/2RCf_{sw}}}{Cf_{sw} (1 - e^{-1/2RCf_{sw}})} = \frac{1}{Cf_{sw}} \quad (2.30)$$

$$R_{FSL} = \lim_{f_{sw} \rightarrow \infty} R_{OUT} = \lim_{f_{sw} \rightarrow \infty} \frac{\frac{\partial}{\partial f_{sw}} \left(\frac{1 + e^{-1/2RCf_{sw}}}{Cf_{sw}} \right)}{\frac{\partial}{\partial f_{sw}} (1 - e^{-1/2RCf_{sw}})} \quad (2.31)$$

$$= \lim_{f_{sw} \rightarrow \infty} \frac{\frac{1}{C} \left(\frac{1}{2RCf_{sw}} e^{-1/2RCf_{sw}} - (1 - e^{-1/2RCf_{sw}}) \right)}{\frac{1}{2RC} e^{-1/2RCf_{sw}}} = 4R. \quad (2.32)$$

L'Hospital's rule is used in (2.32) to complete the derivation. By inspection, these limits to the general output resistance match those calculated in sections 2.1 and 2.2.

The exact output impedance formula may be difficult or impossible to find for many converters, so an approximation would be beneficial for design purposes. Besides simply adding the two impedance components, the output impedance is often approximated as [28]:

$$R_{OUT} \approx \sqrt{R_{SSL}^2 + R_{FSL}^2}. \quad (2.33)$$

These two approximations along with the exact output impedance for this example in (2.29) are plotted in figure 2.8. In this evaluation, $R = C = 1$, but the results are representative of any SC converter. The approximation in (2.33) is reasonably close to the modeled results, and will be used throughout this work.

2.4 Model Simplification for Two-Phase Converters

The majority of well-known SC converter topologies are two-phase converters. Previous analysis [27, 50, 51] only considered two-phase converters, so relating the analysis in sections 2.1 and 2.2 to the two-phase case would be useful and beneficial for the analysis later in this work.

In a two-phase converter, single \mathbf{a}_c and \mathbf{a}_r vectors can be defined. Due to charge conservation, the two capacitor charge multipliers are equal and opposite, such that we can define:

$$\mathbf{a}_c = \mathbf{a}_c^1 = -\mathbf{a}_c^2 \quad (2.34)$$

Similarly, since each switch is on during exactly one phase, an \mathbf{a}_r vector can be made with the non-zero $a_{r,i}^j$ components.

Next, the SSL and FSL output impedance results can be similarly simplified given two phases and the above vector definitions. Additionally, a duty cycle of 50% will be assumed. The SSL impedance in (2.15) can be simplified to:

$$R_{SSL} = \sum_{i \in caps} \frac{(a_{c,i})^2}{C_i f_{sw}} \quad (2.35)$$

Similarly, the FSL impedance in (2.24) can be simplified to:

$$R_{FSL} = 2 \sum_{i \in switches} R_i (a_{r,i})^2 \quad (2.36)$$

These equations simplify the output impedance calculations derived for multi-phase converters. Where generality will be maintained in much of the work, for specific two-phase converters, these terms and formulas will be used instead.

2.5 Modeling Other Converter Loads

The models in the previous sections only consider voltage sources attached to the ports of an SC converter. In real converters, the load is rarely modeled as a voltage source. Numerous additional loads can be applied, the three addressed here include capacitive, inductive

and current-source loads. These other loads either more-typically represent frequently-occurring loads or alternate loads which may improve efficiency.

2.5.1 Capacitive Loads

The most common load of an SC converter is a constant-current or resistive load with a large output (bypass) capacitor. If the output capacitor is sufficiently large, the load appears like a fixed voltage source at the switching frequency. If the size of the output capacitance is limited, a ripple voltage will appear on the output due to the impulsive current transfer occurring in the SSL. The load current discharges this output capacitor linearly between the phase transitions. Since the output capacitor is being discharged by a current source, the impulsive charges delivered to the output capacitor do not add to zero, but instead add to the average output current. Since the losses due to this impulsive charging are related to the square of the magnitude of each charge impulse, the loss is minimized if the impulses are of equal size in each phase. When the charge delivered to the output is equal in each phase, the linear output capacitor's charging loss can be added to the SSL impedance calculation by using a charge multiplier of $1/j$ in each of the j phases. Non-uniform charge transfer increases the loss associated with the output capacitance, but can be reduced by using a converter with multiple interleaved phases. The discharging of the output capacitor due to the load current does not contribute additional loss since it is done adiabatically via the current-source load.

The ripple at the output of a converter can have negative effects on the load (if it consists of sensitive analog or digital circuits) or on the converter's control circuitry. Furthermore, a small output capacitance may have a negative effect on the efficiency of the converter due to the ripple voltage on this capacitance. Output voltage ripple will be further examined in section 5.1.

2.5.2 Current-Source Load

Loads that can be modeled as a current source have a promising use in SC converters. When linear capacitors are charged via voltage sources, as in the above analysis, they lose a substantial fraction of the transfer energy in the charging process, given by

$$E_{LOSS} = \frac{1}{2} \Delta q_c \Delta v_c. \quad (2.37)$$

This loss is directly equivalent to the SSL resistive loss. If the capacitors can be charged via a series current source, the converter could be nearly 100% efficient. Additionally, as efficiency declines with load in the SSL with voltage source charging, the power density of a current-source charged converter can be dramatically improved. Reference [37] describes a two-stage SC-buck converter, where the buck converter provides a current-source-like load for the SC converter. By providing this *soft-charging* ability, the SC converter's loss decreases by 21%.

Figure 2.9a shows a 2:1 ladder converter. In figure 2.9b, the output voltage and flying capacitor voltage are shown for this converter based on both a voltage-source load (representative of a resistor-capacitor load) and a current source load. By charging and discharging the flying capacitor via a current source, a higher efficiency is achieved as the SSL impedance loss is eliminated. However, the output exhibits significant voltage ripple. In many applications, a constraint is often placed on the minimum value of the output voltage to ensure proper operation of the load. For example, in a microprocessor, some instructions may yield incorrect results if the supply voltage drops below the minimum voltage during execution of that instruction. If the minimum of the output voltage is considered, the efficiency of this converter is identical to the voltage source load condition.

2.5.3 Inductive Load

While current source loads have the ability to greatly increase the efficiency of an SC converter, very few real loads provide the boost in efficiency provided by a current source load. However, by using an inductive filter on the output, a similar effect can be obtained.

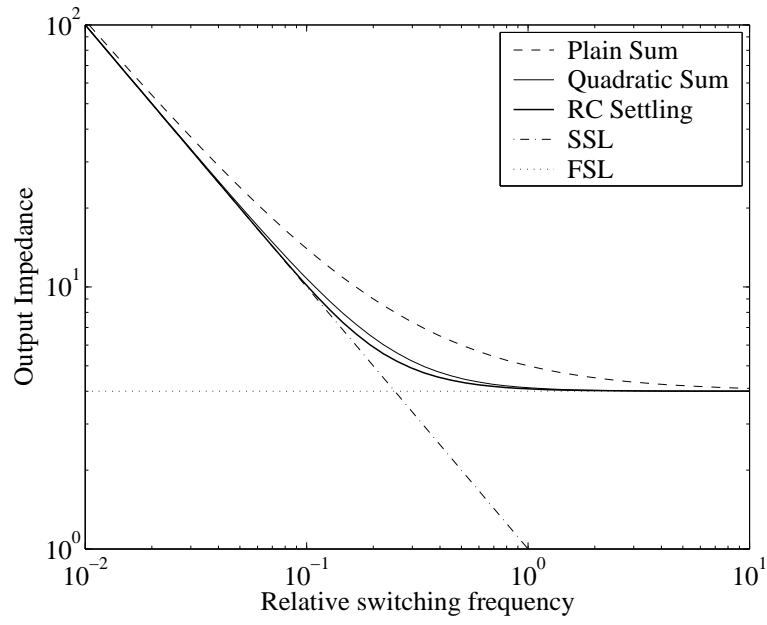


Figure 2.8. Output impedance when $R_{SSL} \approx R_{FSL}$ and approximations

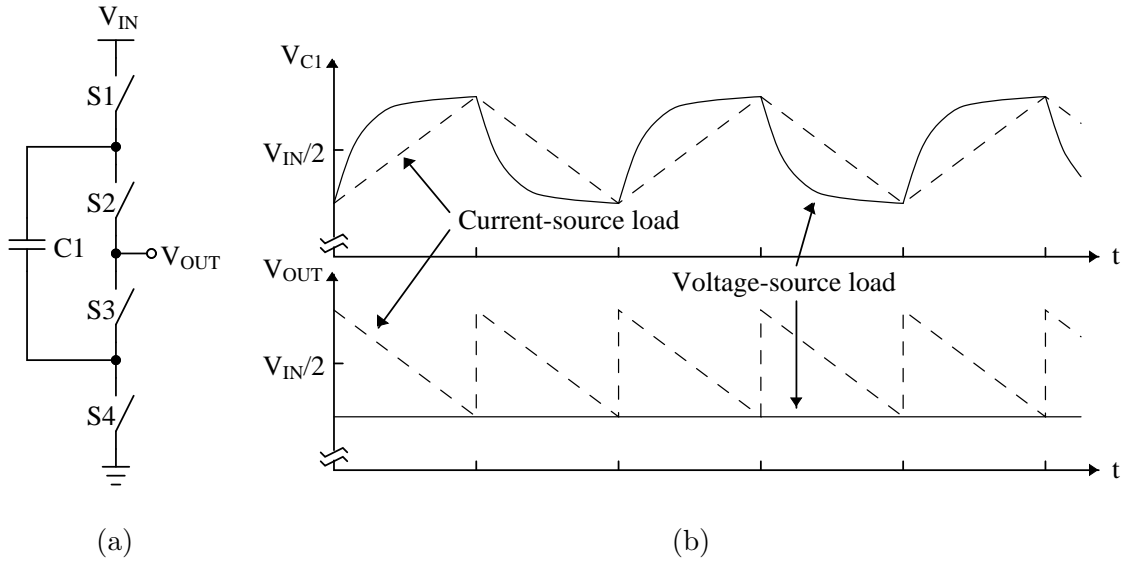


Figure 2.9. 2:1 ladder converter: (a) topology (b) waveforms for current and voltage source loads

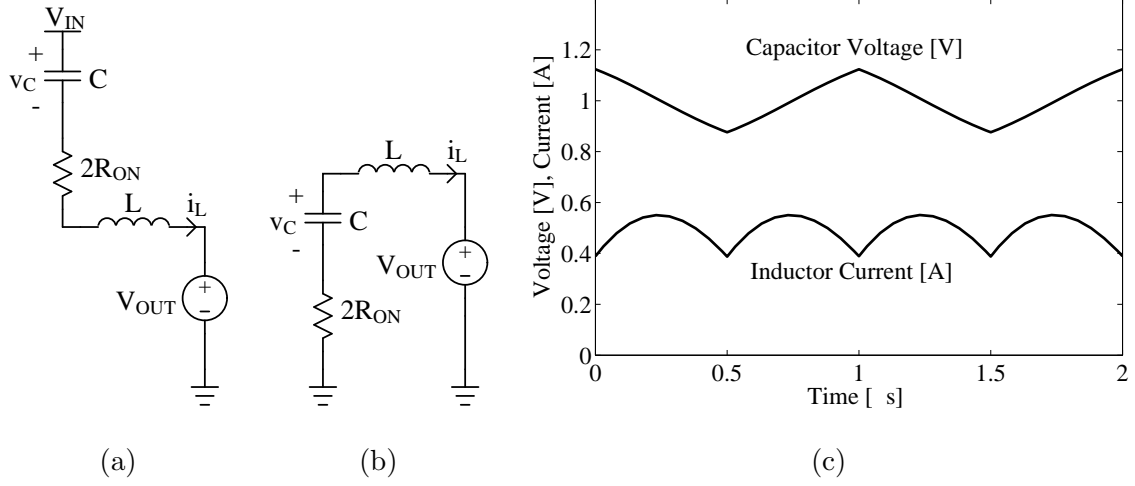


Figure 2.10. SC converter with inductive load: a) phase 1 network, b) phase 2 network, c) waveforms

Since an inductor at the output holds the output current continuous, it acts similar to a current-source load.

Like a current-source load, an inductive load may cause problems for implementation. Since the output current is forced continuous, methods for keeping the current continuous during phase switching events must be implemented. The phase dynamics are now based on a RLC network (not an RC network), so ringing can occur during phase transitions. This ringing can contribute to both additional losses and device stresses. Careful design techniques must be used to prevent the ringing from destroying the transistors when using an inductive load.

Despite the implementation difficulties, using an inductive load may still be beneficial for certain applications. To examine the benefits of using an inductive load, a time-domain analysis of a switching period will be performed using the topology in figure 2.9a with an inductor and DC voltage source at the output. Figures 2.10a and 2.10b show the RC networks formed by the topology in phases 1 and 2, respectively. These two networks can be characterized by a differential equation specific to this topology:

$$\frac{d}{dt}i_L + \frac{R}{L}i_L + \frac{1}{L}v_C = \begin{cases} \frac{1}{L}(V_{IN} - V_{OUT}) & \text{phase 1} \\ \frac{1}{L}(V_{OUT}) & \text{phase 2} \end{cases} \quad (2.38)$$

$$\frac{d}{dt}v_C = \frac{i_L}{C} \quad (2.39)$$

These two RLC networks create symmetric transients during each of the two periods, shown in figure 2.10c. In steady-state operation, the capacitor voltage waveform is symmetric around $V_{IN}/2$, and the inductor current reaches the same value at the end of each phase. These relationships set up two boundary conditions:

$$v_C(T/2) = V_{IN} - v_C(0) \quad (2.40)$$

$$i_L(T/2) = i_L(0) \quad (2.41)$$

When these boundary conditions are used to solve the differential equations for the two phase networks, the steady-state waveforms in figure 2.10c can be reproduced. The voltage change on the capacitor in a single phase is proportional to the output current during that phase. Thus, the output current and output resistance can be found accordingly:

$$I_{OUT} = f_{sw} 4C \left(\frac{V_{IN}}{2} - v_C(0) \right), \quad (2.42)$$

$$R_{OUT} = \frac{\left(\frac{V_{IN}}{2} - V_{OUT} \right)}{I_{OUT}}. \quad (2.43)$$

For a given switching frequency, capacitor values and switch on-state resistance values, it is informative to determine the effect a certain inductance has on the output impedance, and thus converter efficiency. The output impedance, found using the preceding method, is evaluated for a range of inductance values, and is shown in figure 2.11 for three values of switch on-state resistance.

As is clear from figure 2.11, there is a critical inductance (approximately 10 nH in this case) where the SSL output impedance component is eliminated for inductances above the critical value. The critical inductance is given approximately by

$$L_{crit} = \frac{1}{C \sqrt{2\pi f_{sw}}} \quad (2.44)$$

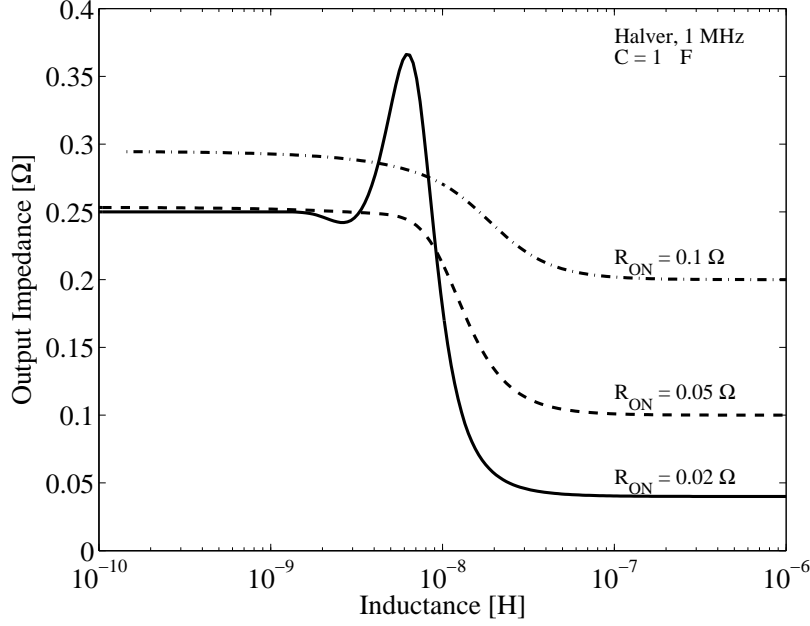


Figure 2.11. Output impedance of SC converter with inductive load

where f_{sw} is the switching frequency and C is the value of the equivalent flying capacitance. The left asymptote corresponds to the voltage source load case, where the SSL and FSL impedance combine to form the converter's output impedance. The right asymptote corresponds to the current-source load case, where the capacitor-related losses are eliminated and the converter's output impedance equals the FSL impedance.

This analysis was performed for a specific converter topology. A similar effect will occur for converters where all capacitors are charged and discharged in series with the output (typically step-down converters). Some topologies (especially step-up topologies) will still exhibit lossy charging or discharging as some current paths do not include the output source.

Additionally, a resonance occurs between the flying capacitors and the output inductor for low values of switch resistance. When the resonance frequency aligns with the switching frequency, little net current can be transferred each period, yielding a higher output impedance. This phenomenon must be avoided if an inductive load is used. However, if the pitfalls of this method are avoided, a small-value inductor at the output of a converter can be used to greatly improve converter efficiency.

Chapter 3

Optimization of Switched-Capacitor Converters

A method of determining the output resistance of switched-capacitor (SC) DC-DC converters was developed in chapter 2. Expressions for evaluating the slow- and fast-switching-limit output impedance were developed in terms of the switching frequency, network arrangement and component parameters. This general and relatively simple analysis method creates an extremely powerful framework for SC converter design. This chapter will discuss the device choices and sizing for each individual component in the SC networks. Based on a cost-based metric, the switches and capacitors of the SC converter can be independently optimized. System design, including choosing the switching frequency and the relative sizing between switches and capacitors, will be discussed in section 3.3.

The optimization procedure requires knowledge of the component working voltages, which was not required for the output impedance analysis. The working voltage for a capacitor is the maximum voltage on the capacitor during steady-state converter operation. For a transistor (switch), the working voltage is the voltage it blocks during steady-state converter operation. For open-circuit operation, these working voltages can be found by inspection in most examples, or by the process outlined in reference [27] or in appendix

A. This analysis is based on combining KVL constraints for the two phase topologies, in combination with a known source voltage. The result is the computation of vectors denoted \mathbf{v}_c and \mathbf{v}_r for the working voltages of the capacitors and switches, respectively, ratioed to the converter output voltage.

3.1 Device Cost Metrics

Before the performance of a converter is optimized, each component in the circuit must be matched with a technology suitable to implement that component. To match a component with a device, a switch performance metric must be evaluated for all available device technologies and the device with the greatest metric value chosen. The first criteria is that the device's blocking voltage, given by $\mathbf{v}_c(\text{rated})$ or $\mathbf{v}_r(\text{rated})$ for capacitors and switches, respectively, must exceed the maximum blocking voltage of the component. It is important to note that during high-load conditions, the blocking voltage of some components may exceed the no-load steady-state condition. Additionally, startup and shutdown circuitry must ensure the transient voltages do not exceed the device ratings.

Next, a cost metric for each device technology must be developed. These metrics must reflect the performance of a device for a given cost. In integrated circuits, this cost is typically die area, but could be power loss in applications where that component is not limiting system area. For capacitors, the performance of a device can be represented as its energy storage as used in the application. Thus, the areal energy density capacitor metric can be given by:

$$M_{cap} = \frac{C v_{c,i}^2}{2 A_{cap}} \quad (3.1)$$

where C is the capacitance of a test device occupying area A_{cap} , and $v_{c,i}$ is the voltage that the capacitor blocks in normal operation. Since capacitance scales linearly with area, this metric is constant for a given technology and component in the topology. Thus, for a given component, the device with the largest metric, while meeting the voltage rating constraint, should be used for the design.

Similarly, the performance of a switch can be represented by its V-A product. The V-A product represents the product of the blocking voltage and FSL on-state current. This V-A product is related to the product between a switch's conductance and the square of its blocking voltage, as described in section 3.2.

The cost of a switch can be represented as its die area, for area-limited integrated applications. If the switch area in an application is not limited (i.e. if the capacitor area dominates the switch area, as in many IC application examples), the cost of a switch can be equated to the switching loss of the device. Thus, the optimization can use one of the following two switch metrics:

$$M_{sw1} = \frac{G v_{r,i}^2}{A_{sw}} \quad (3.2)$$

$$M_{sw2} = \frac{G v_{r,i}^2}{C_G v_{G,i}^2 + C_D v_{r,i}^2 + C_{BS} v_{B,i}^2} \quad (3.3)$$

where G is the on-state conductance of the test switch of area A_{sw} , and $v_{r,i}$ is the blocking voltage of switch i in the topology. The switch metric represents the ratio between the performance of the switch, given by the G - V^2 product, and the cost of a switch, given by either die area or capacitive switching loss. The metrics in (3.2) and (3.3) have different units, representing the units of their respective costs, and must be used in an optimization specific to that cost. In (3.3), C_G , C_D and C_{BS} are the linearized gate, drain and source-body capacitances of the test switch, respectively. The voltages $v_{G,i}$, $v_{r,i}$ and $v_{B,i}$ are the peak-to-peak amplitudes of the gate-source, drain-source and body-source voltages, respectively. When choosing a device technology for each component, the device with the largest relevant metric, while having a sufficiently-high rated voltage, should be used for a given component in the topology.

3.2 Component Sizing

Now that a method has been developed to choose the best device technology available for each given component, each component must be sized relative to each other to obtain

the best performance for a given total device area or parasitic power loss. Given that the losses attributed to ideal capacitors and resistive switches are reflected in the computation of a single real output resistance, the components can now be optimized to minimize that output impedance. Minimal output impedance corresponds to maximum efficiency for a given power delivered, and dually, corresponds to maximum power delivery for a given loss. This section develops optimality computations for the slow switching limit (SSL) and fast switching limit (FSL) impedances. When optimizing over capacitances, one should minimize the output impedance that is associated only with the capacitances, namely the SSL impedance found in section 2.1. Analogously, when optimizing over switch sizes, one should minimize the FSL output impedance found in section 2.2.

While the optimization can be carried out for each of the metrics in section 3.1, for sake of brevity, the derivation will be shown for an idealized device metric as follows, and the results using each metric will be shown in tables 3.1 and 3.2. For capacitors, their area (or volume) is typically related to their maximum possible energy storage. Thus, the following optimization will hold total capacitor energy storage constant using this constraint:

$$E_{tot} = \sum_{i \in caps} \frac{1}{2} C_i (v_{c,i(rated)})^2. \quad (3.4)$$

The energy storage cost of a capacitor is related to its rated voltage, not the maximum voltage it sees during operation.

The switches' areal cost metric can be idealized to a constraint on the total V-A product summed across all the switches in the converter. As proposed in section 3.1, the V-A product corresponds to the product between a switch's conductance and the square of its blocking voltage as described here. This G-V² constraint can be represented as:

$$X_{tot} = \sum_{i \in switches} G_i (v_{r,i(rated)})^2. \quad (3.5)$$

This V-A product is related to the product between a switch's conductance and the square of its blocking voltage, for both discrete and integrated switches. Paralleling switches increases total conductance, whereas placing switches in series increases voltage blocking while decreasing conductance. To increase voltage blocking without reducing conductance,

the number of devices used scales quadratically, motivating the G-V² metric. In an integrated application, the same total G-V² constraint applies. Roughly, the transistor length and nominal voltage scale linearly with process feature size. In addition, switch conductance scales proportionally with transistor width and inversely with transistor length.

3.2.1 Capacitor Sizing

To optimize relative capacitor sizes, a Lagrange multiplier method will be used for the equality-constrained optimization problem. The SSL output impedance (2.15) will be minimized while the constraint on total energy (3.4) will be held constant. A function \mathcal{L} is defined to perform the constrained optimization:

$$\mathcal{L} = \sum_{i \in caps} \sum_{j=1}^n \frac{(a_{c,i}^j)^2}{2C_i} + \lambda \left(\sum_i \frac{1}{2} (v_{c,i(rated)})^2 C_i - E_{tot} \right) \quad (3.6)$$

where the first term represents the SSL output impedance (scaled by switching frequency as it does not affect the minimization) and the second term incorporates the energy constraint in (3.4). The impedance is minimized by equating the partial derivatives of \mathcal{L} with respect to both C_i and λ with zero:

$$\frac{\partial \mathcal{L}}{\partial C_i} = - \sum_{j=1}^n \frac{(a_{c,i}^j)^2}{2C_i^2} + \lambda \frac{1}{2} (v_{c,i(rated)})^2 = 0 \quad (3.7)$$

$$\frac{\partial \mathcal{L}}{\partial \lambda} = \sum_i \frac{1}{2} (v_{c,i(rated)})^2 C_i - E_{tot} = 0 \quad (3.8)$$

Note that equation (3.8) simply repeats the constraint in (3.4).

The relationship in (3.7) sets up a proportionality between C_i , $a_{c,i}^j$ and $v_{c,i(rated)}$. The energy constraint can be used to find an expression for the value of each capacitor:

$$C_i = \frac{\sqrt{\sum_{j=1}^n (a_{c,i}^j)^2}}{v_{c,i(rated)}} \frac{2 E_{tot}}{\sum_{k \in caps} v_{c,k(rated)} \sqrt{\sum_{j=1}^n (a_{c,k}^j)^2}} \quad (3.9)$$

The optimal energy storage rating of each capacitor is proportional to the V-Q product of each capacitor:

$$E_i = \frac{v_{c,i}(\text{rated}) \sqrt{\sum_{j=1}^n (a_{c,i}^j)^2}}{\sum_{k \in \text{caps}} v_{c,k}(\text{rated}) \sqrt{\sum_{j=1}^n (a_{c,k}^j)^2}} E_{tot} \quad (3.10)$$

When the total energy is constrained, the optimal capacitor energies are proportional to the product of their rated voltage and their charge multiplier coefficients. In addition, the ripple voltage on each capacitor is directly proportional to that capacitor's rated voltage.

The optimized output impedance can be calculated by combining (2.15) and (3.9):

$$R_{SSL}^* = \frac{1}{4E_{tot}f_{sw}} \left(\sum_{i \in \text{caps}} v_{c,i}(\text{rated}) \sqrt{\sum_{j=1}^n (a_{c,i}^j)^2} \right)^2 \quad (3.11)$$

Since many commonly-used SC topologies use only two phases, it is useful to simplify the results in (3.9) and (3.11) using the relation $a_{c,i} = a_{c,i}^1 = -a_{c,i}^2$. The optimized capacitor values and total SSL output impedance for a two-phase SC converter are given by:

$$C_i = \left| \frac{a_{c,i}}{v_{c,i}(\text{rated})} \right| \frac{2E_{tot}}{\sum_k |a_{c,k} v_{c,k}(\text{rated})|} \quad (3.12)$$

$$R_{SSL}^* = \frac{1}{2E_{tot}f_{sw}} \left(\sum_{i \in \text{caps}} |a_{c,i} v_{c,i}(\text{rated})| \right)^2 \quad (3.13)$$

By optimizing the capacitors, the output impedance becomes proportional to the square of the sum of the products of voltages and charge flows (V-A product) of each capacitor. This optimization can improve the performance of an SC converter designed in an ad-hoc manner significantly, especially one with a large conversion ratio. For example, if a high-ratio ladder converter is designed, using this method to size the capacitors will yield a significant performance advantage over the converter if uniform capacitor sizes were used instead.

3.2.2 Switch Sizing

Like capacitors, the switches in a SC converter can be optimized, yielding dramatic performance increases. This optimization is carried out in the asymptotic fast switching limit where output impedance is directly related to switch conductance. Similar to the SSL optimization case, a Lagrange optimization function \mathcal{L} is formed to minimize the FSL output impedance while satisfying the constraint in (3.5):

$$\mathcal{L} = \sum_i \sum_{j=1}^n \frac{(a_{r,i}^j)^2}{G_i} + \lambda \left(\sum_{i \in \text{switches}} G_i (v_{r,i}(\text{rated}))^2 - X_{tot} \right) \quad (3.14)$$

The first term corresponds to the FSL output impedance (the omission of the factor of the number of phases denoted by n in (2.24) does not affect the optimization) and the second term corresponds to the constraint in (3.5). The minimization is performed by taking the partial derivative of (3.14) with respect to G_i and setting it to zero:

$$\frac{\partial \mathcal{L}}{\partial G_i} = - \sum_{j=1}^n \frac{(a_{r,i}^j)^2}{G_i^2} + \lambda (v_{r,i}(\text{rated}))^2 = 0 \quad (3.15)$$

Again, differentiating (3.14) with respect to λ yields the constraint in (3.5).

Manipulating equation (3.15) yields a proportionality between G_i and the ratio between the switch's charge multiplier coefficient and its voltage rating. This proportionality, when combined with the G-V² constraint in (3.5), yields an expression for the optimal conductance of each switch:

$$G_i^* = \frac{1}{R_i^*} = \frac{\sqrt{\sum_{j=1}^n (a_{r,i}^j)^2}}{v_{r,i}(\text{rated})} \frac{X_{tot}}{\sum_k v_{r,k}(\text{rated}) \sqrt{\sum_{j=1}^n (a_{r,k}^j)^2}} \quad (3.16)$$

Comparing the optimal conductance G_i to the optimal capacitance in (3.9) makes it evident that the two optimizations are analogous.

The optimal FSL output impedance is obtained by substituting (3.16) into (3.17):

$$R_{FSL}^* = \frac{n}{X_{tot}} \left(\sum_i v_{r,i}(\text{rated}) \sqrt{\sum_{j=1}^n (a_{r,i}^j)^2} \right)^2 \quad (3.17)$$

where n is the number of phases used.

Since most of the commonly-used topologies use two phases, for the two-phase case, the optimized switch conductance in (3.16) and the optimized FSL output impedance in (3.17) can be simplified to:

$$G_i^* = \frac{1}{R_i^*} = \left| \frac{a_{r,i}}{v_{r,i(rated)}} \right| \frac{X_{tot}}{\sum_k |a_{r,k} v_{r,k(rated)}|} \quad (3.18)$$

$$R_{FSL}^* = \frac{2}{X_{tot}} \left(\sum_i |a_{r,i} v_{r,i(rated)}| \right)^2. \quad (3.19)$$

Similar to the optimal SSL impedance, the optimal FSL output impedance is related to the square of the sum of the V-A products. This simple form of the optimal output impedance allows the comparison of various SC converter topologies, as performed in chapter 4.

3.2.3 Optimizing Using Other Metrics

Sections 3.2.1 and 3.2.2 present a method to optimize the relative capacitor and switch sizing, respectively, in an SC converter. However, the optimization is performed assuming limits on capacitor energy storage and switch V-A product. If varied device technologies are used, a more practical cost metric must be used. This optimization can also be performed using the metrics developed in section 3.1, namely the die area and parasitic power loss metrics. The detailed optimization using these metrics will not be shown here, since it is nearly identical to the derivation in sections 3.2.1 and 3.2.2. The results of the optimizations, including the relevant constraints, component sizing, and output impedance, are shown in table 3.1 for the capacitor optimization and in table 3.2 for the switch optimization.

	General Cost	Area-based Cost
Device Cost	Energy storage	Die area
Cost Constraint	$E_{tot} = \sum_i \frac{1}{2} C_i (v_{c,i}(rated))^2$	$A_{tot} = \sum_i A_i$
Device Metric	N/A	$M_{cap} = \frac{C_i (v_{c,i}(rated))^2}{2A_{cap}}$
Optimized Capacitor Values	$C_i^* = \left \frac{a_{c,i}}{v_{c,i}(rated)} \right \left \frac{2E_{tot}}{\sum_k a_{c,k} v_{c,k}(rated) } \right $	$C_i^* = \left \frac{a_{c,i}}{v_{c,i}(rated)} \right \sqrt{M_{cap,i}} \frac{2A_{tot}}{\sum_k \frac{ a_{c,k} v_{c,k}(rated) }{\sqrt{M_{cap,k}}}}$
Optimized Output Impedance	$R_{SSL}^* = \frac{1}{2E_{tot} f_{sw}} (\sum_i a_{c,i} v_{c,i}(rated))^2$	$R_{SSL}^* = \frac{1}{2A_{tot} f_{sw}} \left(\sum_i \frac{ a_{c,i} v_{c,i}(rated) }{\sqrt{M_{cap,i}}} \right)^2$

Table 3.1. Capacitor optimization summary for two device cost bases (two-phase simplifications)

39

	General Cost	Area-based Cost	Loss-based Cost
Device Cost	V-A Product	Die area	Parasitic-capacitance loss
Cost Constraint	$X_{tot} = \sum_i G_i (v_{r,i}(rated))^2$	$A_{TOT} = \sum_i A_i$	$E_{loss} = \sum_i C_G v_{G,i}^2 + C_D v_{r,i}^2 + C_B v_{B,i}^2$
Device Metric	N/A	$M_{sw1,i} = \frac{G_i (v_{r,i}(rated))^2}{A_{sw}}$	$M_{sw2,i} = \frac{G_i (v_{r,i}(rated))^2}{C_G v_{G,i}^2 + C_D v_{r,i}^2 + C_B v_{B,i}^2}$
Optimized Switch Conductances	$G_i^* = \left \frac{a_{r,i}}{v_{r,i}(rated)} \right \left \frac{X_{tot}}{\sum_k a_{r,k} v_{r,k}(rated) } \right $	$G_i^* = \left \frac{a_{r,i}}{v_{r,i}(rated)} \right \frac{A_{tot} \sqrt{M_{sw1,i}}}{\sum_k \frac{ a_{r,k} v_{r,k}(rated) }{\sqrt{M_{sw1,k}}}}$	$G_i^* = \left \frac{a_{r,i}}{v_{r,i}(rated)} \right \frac{E_{loss} \sqrt{M_{sw2,i}}}{\sum_k \frac{ a_{r,k} v_{r,k}(rated) }{\sqrt{M_{sw2,k}}}}$
Optimized Output Impedance	$R_{FSL}^* = \frac{2}{X_{tot}} (\sum_i a_{r,i} v_{r,i}(rated))^2$	$R_{FSL}^* = \frac{2}{A_{tot}} \left(\sum_i \frac{ a_{r,i} v_{r,i}(rated) }{\sqrt{M_{sw1,i}}} \right)^2$	$R_{FSL}^* = \frac{2}{E_{loss}} \left(\sum_i \frac{ a_{r,i} v_{r,i}(rated) }{\sqrt{M_{sw2,i}}} \right)^2$

Table 3.2. Switch optimization summary for two device cost methods (two-phase simplifications)

Tables 3.1 and 3.2 show the form of the cost constraint, the specific device metrics, the optimized device values and optimized output impedance of an SC converter for specific cost metrics. The general cost columns corresponds to the idealized $G\text{-}V^2$ cost metric which can be used for technology-independent converter designs or designs involving only a single device technology. If a different device metric must be used to account for varying device technologies, the area-based costs and loss-based cost columns show the specific optimization details for these specialized cost metrics.

The results shown in tables 3.1 and 3.2 show some general patterns about optimizing SC converters. First, capacitance and conductance are analogous in the SSL and FSL calculations, respectively. The value of each component (capacitance or conductance) is proportional to the ratio between its charge multiplier and its rated blocking voltage. Additionally, if a specific cost metric is used, each component value is proportional to the square root of that device cost metric. The die area of each component (or whichever cost corresponds to the method used) is proportional to the charge multiplier and blocking voltage, and proportional to the square root of the device's cost metric.

As an example, if an integrated SC converter was made using NMOS and PMOS transistors, either the area-based or loss-based cost metric can be used. Since the performance of PMOS devices is typically inferior to that of NMOS devices, PMOS devices would exhibit a device metric equal to approximately half of the metric of NMOS devices. Thus, for a converter with all identical switch charge multipliers, the optimally-sized PMOS devices would be larger than the NMOS devices by a factor of the square-root of two, but their conductances would be less than the conductance of the NMOS devices by the same square-root of two factor.

This general component-size optimization can be extended to any device metric as desired. It gives a powerful method to size the individual capacitors and switches of an SC converter and provides substantial insight into its operation and performance. However, to yield an optimally-performing converter, the proper ratio of capacitance to switch size must be chosen, as well as the switching frequency. Section 3.3 performs this optimization con-

sidering the system-wide tradeoffs between switching frequency, capacitor area and switch area.

3.3 System-Level Converter Optimization

In section 3.2, the sizing of individual capacitors and switches in an SC converter was optimized independently. However, it is also critical to choose a total capacitor area, switch area and switching frequency to globally optimize the converter. In this section, total converter performance will be optimized for a given design point. A design point consists of a specific output current I_{OUT} and input voltage V_{IN} . To examine a converter's performance over a range of currents and for a specific output voltage, the converter's control method must be also examined. Chapter 5 goes into further depth concerning issues relating to regulation of SC converters.

In integrated circuit implementations, there are three design parameters. Parameter A_{SW} is the die area of the transistors, including drain and source regions and accounting for appropriate design rules. Since switch area is measured in mm^2 , the switch-area cost metric will be used in this optimization. Similarly, A_C is the die area of the capacitors, measured in mm^2 . The capacitor area cost metric should be used in this case, adjusting capacitor density to account for density rules and contact areas. The final design parameter is the switching frequency f_{SW} , measured in hertz. This optimization method can be easily adapted for discrete implementations if desired. Such an optimization method was used in reference [33] to design a discrete-capacitor converter.

3.3.1 Converter Loss Components

The optimization method will be performed by evaluating and minimizing the total power loss for the given design point with a constraint placed on capacitor area. Five loss components will be evaluated as part of this power loss. The first loss, the *SSL impedance loss* is due to the power loss in the component of the output impedance related to charge

transfer. The basis of the SSL loss is explained in section 2.1. This component of loss can be expressed as:

$$P_{SSL} = I_{OUT}^2 \frac{1}{2A_C f_{sw}} \left(\sum_i \frac{|a_{c,i} v_{c,i} (rated)|}{\sqrt{M_{cap,i}}} \right)^2 \quad (3.20)$$

where the optimized output impedance using die-area-based cost metrics is used. The two-phase simplification for the impedance components is used in this section, but the multiphase results can be easily substituted.

The second loss is the *FSL impedance loss*, which is similarly the power loss due to the FSL output impedance, described in section 2.2. Using the die-area-based cost metric, the FSL impedance loss can be written as:

$$P_{FSL} = I_{OUT}^2 \frac{2}{A_{SW}} \left(\sum_i \frac{|a_{r,i} v_{r,i} (rated)|}{\sqrt{M_{sw1,i}}} \right)^2. \quad (3.21)$$

With these two loss factors, it is important to note that they are only exact for operation in the SSL and FSL asymptotes, respectively. As discussed in section 2.3, a simple addition of the two loss factors overestimates the total loss. When the SSL and FSL losses are comparable, they will be combined using the Euclidean norm approximation, given by (2.33), in this section.

The final three losses are associated with various parasitics in the converter. First, the drain, gate and body capacitances of the transistors make up the switching loss of the converter. This loss component can be represented as:

$$P_{SW} = f_{sw} \sum_{i \in sw} (C_{G,i} v_{G,i}^2 + C_{D,i} v_{r,i}^2 + C_{B,i} v_{B,i}^2) \quad (3.22)$$

where $C_{G,i}$, $C_{D,i}$ and $C_{B,i}$ are the linearized gate, drain and source-ground (body) capacitance of switch i , respectively. This loss is the basis of the loss-based cost metric used in the device size optimization in section 3.2.3. Since each of the three parasitic capacitances are proportional to the total switch size, the parasitic switch loss is proportional to both switch size and switching frequency.

The second related parasitic loss is due to the bottom-plate parasitic capacitance of the capacitors. This parasitic capacitance is non-negligible for only integrated capacitors, and

represents the capacitance between the physical bottom plate of a metal capacitor and the substrate, or for MOS capacitors, the junction capacitance between the source and drain and the substrate. In this model, the top plate capacitance, if it exists, will be lumped with the bottom-plate capacitance. If the ratio between the parasitic capacitance and the main capacitance is denoted α , the bottom-plate loss can be written as:

$$P_{CAP} = f_{sw} A_C M_{cap} \alpha \frac{V_{C,B}^2}{v_{c(rated)}^2} \quad (3.23)$$

where M_{CAP} is the areal capacitor density metric developed in section 3.1 and $M_{CAP}/v_{c(rated)}^2$ represents the average capacitor density of the capacitors used. The term $V_{C,B}^2$ is the squared-average voltage swing of the bottom-plate voltage of the capacitors, represented by:

$$V_{C,B}^2 = \sum_{i \in caps} \frac{A_{c,i}}{A_{tot}} v_{cb,i}^2 \quad (3.24)$$

where $A_{c,i}$ is the area associated with capacitor i , A_{tot} is the total die area allocated for capacitors, and $v_{cb,i}$ is the magnitude of the bottom-plate swing voltage of capacitor i .

The final loss is the equivalent series resistance (ESR) loss. This loss is a combination of the resistive losses in the capacitors and metal wiring, as switch resistive loss is already considered. This analysis will model that loss as fixed, as it is not obviously related to capacitor or switch area. The loss is given by:

$$P_{ESR} = I_{OUT}^2 R_{ESR} \quad (3.25)$$

where R_{ESR} is an equivalent resistance equal to the sum of the parasitic resistance components, weighted by the square of the ratio between the current flowing through each resistance to the output current. This method of computing the ESR loss is very similar to determining the FSL output impedance in terms of weighting individual resistance components.

3.3.2 Numerical Optimization

To find the global optimal design, these five losses can be evaluated over the design space (the three variables A_{SW} , A_C and f_{sw}). Based on these losses, the efficiency of the

converter can be evaluated. The point which offers the highest efficiency is the optimal and should be the target design point. In many applications, a minimum output voltage is also important, so an additional constraint can be formulated based on the output impedance.

Finding the optimal point in the design space can be accomplished analytically, but the equations will quickly become unmanageable unless drastic simplifications are taken. Thus, this analysis will be performed numerically via a MATLAB program developed as part of this work and described in appendix B. The plots in this section are created using this MATLAB package.

In SC converters where both the switches and capacitors are integrated onto a CMOS IC, capacitor area becomes the primary constraint in converter performance. Thus, the optimal capacitance is the largest available, and thus will be considered as an exogenous variable in this optimization. The total loss of the converter is evaluated over the two-dimensional space of f_{sw} (on the x-axis) and A_{SW} (on the y-axis). The efficiency of an SC converter is given by:

$$\eta = \frac{V_{OUT}I_{OUT}}{V_{OUT}I_{OUT} + P_{LOSS}} \quad (3.26)$$

where P_{LOSS} is the total power loss given by:

$$P_{LOSS} = \sqrt{P_{FSL}^2 + P_{SSL}^2} + P_{SW} + P_{CAP} + P_{ESR}. \quad (3.27)$$

Equation (3.27) uses the square-root approximation to the total output impedance as described in section 2.3.

Figure 3.1 shows a contour plot of the efficiency of an example converter with curves of constant efficiency, when evaluated over the design space. The space is divided into five regions, each denoting the region where each of the five losses is dominant. The optimal point is shown as the circle near the center of the plot. This contour plot illustrates the performance of a converter, but additionally provides insight into the limiting loss factor of the converter and where improvements can be made. Since capacitor area is always a limiting factor in integrated converters, the optimal point will always lie in the SSL loss region. In figure 3.1, as the optimal point borders the SSL loss region and the ESR loss

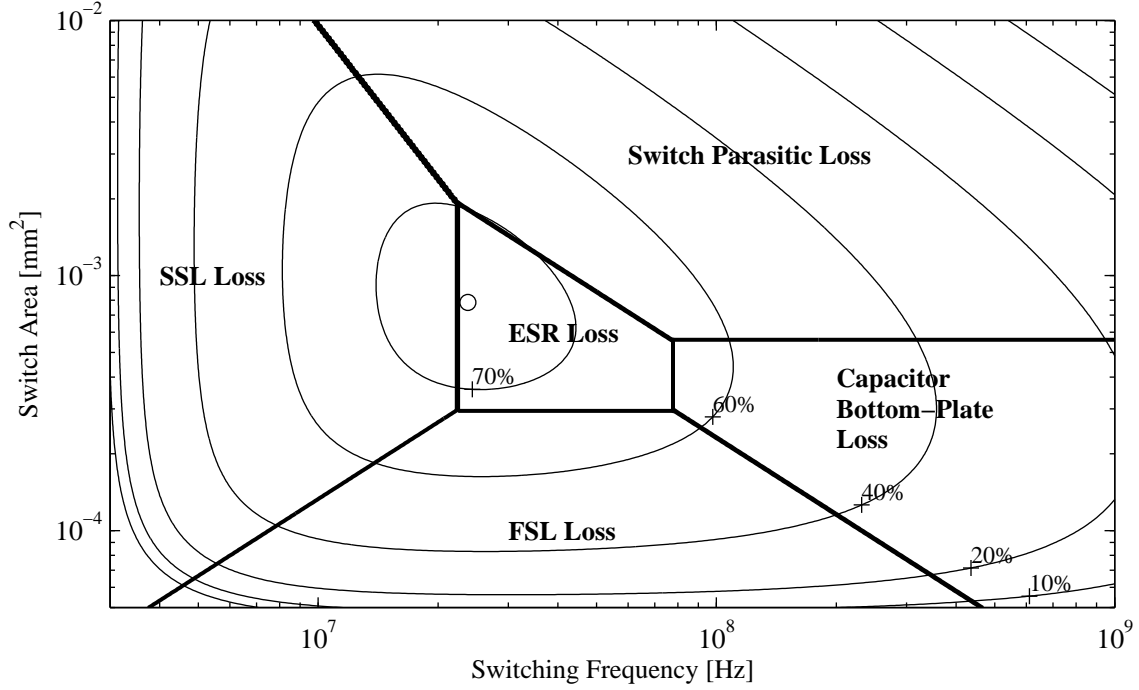
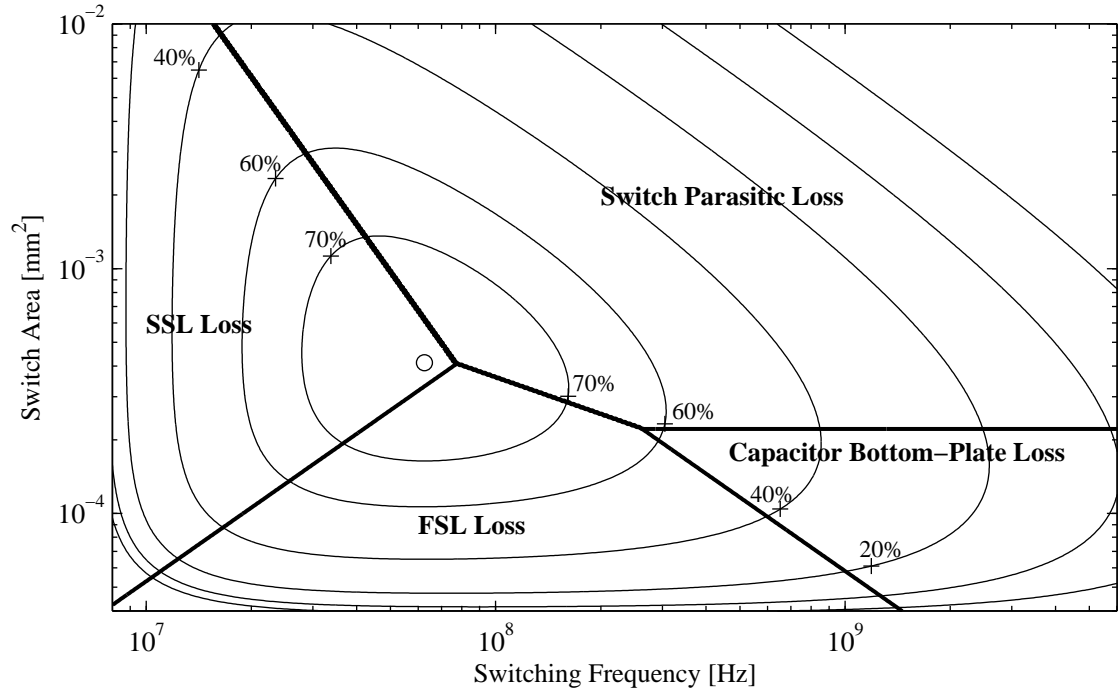


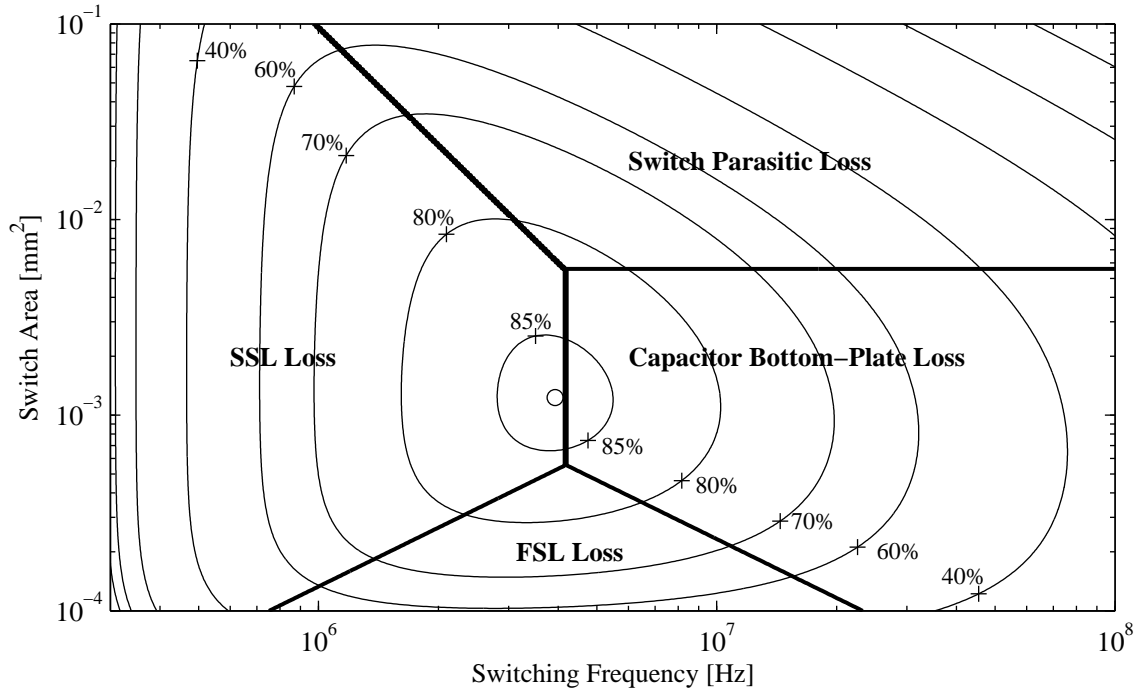
Figure 3.1. Example SC converter optimization plot

region, the metal ESR is the next-dominant loss factor. Improving the switches will only affect the efficiency by a small amount.

Figure 3.2 shows two example contours illustrating different dominant losses. Both of these plots are based on a 3:1 series-parallel converter, discussed in section 4.2.4, designed in a 130 nm CMOS process with metal-insulator-metal (MIM) capacitors. The converter output is nominally 0.4 V (from an input of 1.2 V) at an output current of 5 mA. Figure 3.2a shows the design optimization using 0.4 mm² of capacitor area. The optimal design point is 77% efficient at a switching frequency of about 60 MHz and switch area of 400 μm^2 . The FSL loss and switch parasitic loss regions border the optimal point, along with the SSL impedance loss region. Thus, approximately two-thirds of the converter loss can be associated with the switches. The converter's efficiency can be improved by reducing switch parasitics or otherwise improving switch performance, such as using a smaller gate-length process. Additionally, more capacitor area can be used to reduce the switching frequency, and thus switch loss.



(a) switch-limited design



(b) bottom-plate parasitic capacitance limited design

Figure 3.2. Example efficiency contour plots of a 3:1 series-parallel converter

Figure 3.2b shows the same converter designed with the capacitor area increased to 10 mm². The optimal design is 86% efficient at a switching frequency of 4 MHz, using a switch area of approximately 1200 μm^2 . By increasing the capacitor area by a factor of 25, the switching frequency is reduced by a similar multiple. Since the effects of switch parasitics are significantly reduced, switch area can be increased to reduce the on-state resistance (FSL) loss. The optimal point now borders the SSL loss and capacitor bottom-plate loss regions. Thus, improving switch technology or increasing capacitor area will do little to improve converter efficiency. If efficiency is to be improved, methods to reduce the bottom-plate parasitic capacitance of the MIM capacitors, or to recover some of the charge stored on this capacitance must be used.

By numerically evaluating the five primary losses of an SC converter over the design space, a graphical analysis method is developed to optimize the performance of a SC converter. Besides finding the optimal design point, the graphical method develops intuition in the loss factors of a converter and methods of improving the efficiency. By first ensuring optimal sizing of individual components and then performing a system-wide optimization, a fully optimal converter can be developed for any application.

Chapter 4

Comparing Switched-Capacitor Topologies

In chapter 3, a method was developed to both optimally size the individual components of a switched-capacitor (SC) converter and to pick the correct switch size and switching frequency for maximum efficiency. However, the choice of topology has so far been presumed as given. Choosing the correct topology for a given application and technology is key to an efficient converter.

This chapter develops metrics to compare the performance of different converter topologies. Next, a number of converters in the literature are compared using the general metrics developed. Since the technology used to implement a converter has a large role in determining the best topology, a look at the compatibility between topology choice and device technology is also examined. The performance of switched-capacitor converters is compared to traditional inductor-based converters, showing that SC converters are optimal in many applications. Finally, fundamental limits on the performance of both SC and inductor-based power converters are derived, yielding some powerful insight on the fundamental properties of SC converters.

4.1 Converter Performance Metrics

In order to compare the performance of different converter topologies, a few metrics for converter performance must be developed. Since the comparisons in this chapter are not tied to a particular technology or implementation, the metrics developed here use the V-A product-based component optimization in section 3.2. Two metrics will be developed and used, one for the slow-switching limit (SSL) where a converter's SSL output impedance is examined, and another for the fast-switching limit (FSL) where a converter's FSL output impedance is used.

Each converter metric compares the power handled by a converter to the sum of the energy- or V-A-based device metrics. The power that can be extracted from an SC converter is inversely proportional to its output impedance, and for a constant output impedance, proportional to the square of the output voltage. Thus, the converter's G-V² product is used to represent its power handling capability.

The SSL converter metric is given by:

$$M_{SSL} = \frac{V_{OUT}^2 / R_{SSL}}{f_{sw} \sum_{i \in caps} C_i v_{c,i}^2 / 2} \quad (4.1)$$

where V_{OUT} is the nominal output voltage of the converter and R_{SSL} is the optimized SSL output impedance of the converter, as derived in section 3.2.1. The denominator of the metric is simply the product between the switching frequency of the converter and the total energy storage of the capacitors used.

Analogously, the FSL converter metric can be written as

$$M_{FSL} = \frac{V_{OUT}^2 / R_{FSL}}{\sum_{i \in switches} G_i v_{r,i}^2} \quad (4.2)$$

where R_{FSL} is the optimized FSL output impedance of the converter, as derived in section 3.2.2. The denominator of (4.2) is simply the sum of the G-V² products of the switches used in the converter.

In order to quickly evaluate the performance of converter topologies, the converter metrics will be evaluated in terms of the charge multipliers and blocking voltages. The

multiphase optimized output impedances, in (3.11) and (3.17), will be substituted into the SSL and FSL metrics, given by (4.1) and (4.2), respectively. Through this substitution, the multiphase converter metrics can be expressed as:

$$M_{SSL} = \frac{4 V_{OUT}^2}{\left(\sum_{i \in caps} v_{c,i} (rated) \sqrt{\sum_{j=1}^n \left(a_{c,i}^j \right)^2} \right)^2} \quad (4.3)$$

and

$$M_{FSL} = \frac{V_{OUT}^2}{n \left(\sum_{i \in sw} v_{r,i} (rated) \sqrt{\sum_{j=1}^n \left(a_{r,i}^j \right)^2} \right)^2} \quad (4.4)$$

for the SSL and FSL, respectively. Since the component rated voltages are typically proportional to the output voltage, this metric is independent of voltage level and is just related to the charge multipliers and the ratio of the component voltages.

Since the converters compared in this section are all two-phase topologies, the SSL and FSL metrics in (4.3) and (4.4) can be simplified for a two-phase topology. The two-phase SSL and FSL converter metrics are:

$$M_{SSL} = \frac{2 V_{OUT}^2}{\left(\sum_{i \in caps} |a_{c,i} v_{c,i} (rated)| \right)^2} \quad (4.5)$$

and

$$M_{FSL} = \frac{V_{OUT}^2}{2 \left(\sum_{i \in sw} |a_{r,i} v_{r,i} (rated)| \right)^2} \quad (4.6)$$

respectively.

These two unitless converter metrics can be used to compare SC topologies at different conversion ratios in the switch-limited and capacitor-limited design spaces. Additionally, the metrics can be extended towards inductor-based converters to enable a direct comparison between inductor-based and SC DC-DC converters.

4.2 Analysis of SC Topologies

Two metrics have been developed in section 4.1 to compare the performance of various SC topologies in both the SSL and FSL. In this section, five SC topologies will be compared,

as shown in figure 4.1. The step-up versions of the converters will be examined here, but the step-down converters with the reciprocal conversion ratio exhibit the same performance as the step-up versions. In general, a conversion ratio of $1:n$ will be considered, where n is an integer. Ladder and series-parallel topologies can be created for a general $m : n$ conversion, so for those topologies, a rational conversion ratio will be considered.

In the following sections, the capacitor and switch charge multipliers and blocking voltages for each topology are found. For this analysis, an input voltage of 1 V is assumed, so the v_c and v_r numbers found are the ratio between the blocking voltage and the input voltage. The charge multipliers and blocking voltages found in the following sections will be substituted into (4.3) and (4.4) to find the SSL and FSL converter metrics, respectively.

4.2.1 Ladder Topology

The ladder topology [25] is based on two sets (or ladders) of capacitors. In the analysis of the ladder topology, a general $m : n$ conversion ratio is assumed. For example, figure 4.2 shows a ladder converter with a 2:5 conversion ratio. One set of capacitors forms a chain from ground (including the input and output voltage sources). These capacitors establish a set of DC potentials at integer multiples of the input voltage divided by the conversion ratio denominator m . The other set of capacitors (referred to as the flying capacitors) shuttle charge between the DC-referenced capacitors to equalize them. The switches are phased alternately (odd-numbered switches in phase one, even numbered switches in phase two) to connect the flying capacitors to the DC capacitors.

The capacitor charge multipliers will be found first, followed by the switch charge multipliers. By inspection, C7 in figure 4.2 has a charge multiplier of $|a_{c,7}| = 1$ as it shuttles charge to the output during phase one. In phase two, the charge from C7 charges C6, causing capacitor C6 to have a charge multiplier of magnitude 1, but with an opposite sign to the charge multiplier of C7. The charge multipliers of the capacitors between the input and output can be found by inspection at each junction. This method yields:

$$|a_{c,7}| = |a_{c,6}| = 1 \quad |a_{c,5}| = |a_{c,4}| = 2 \quad |a_{c,3}| = 2. \quad (4.7)$$

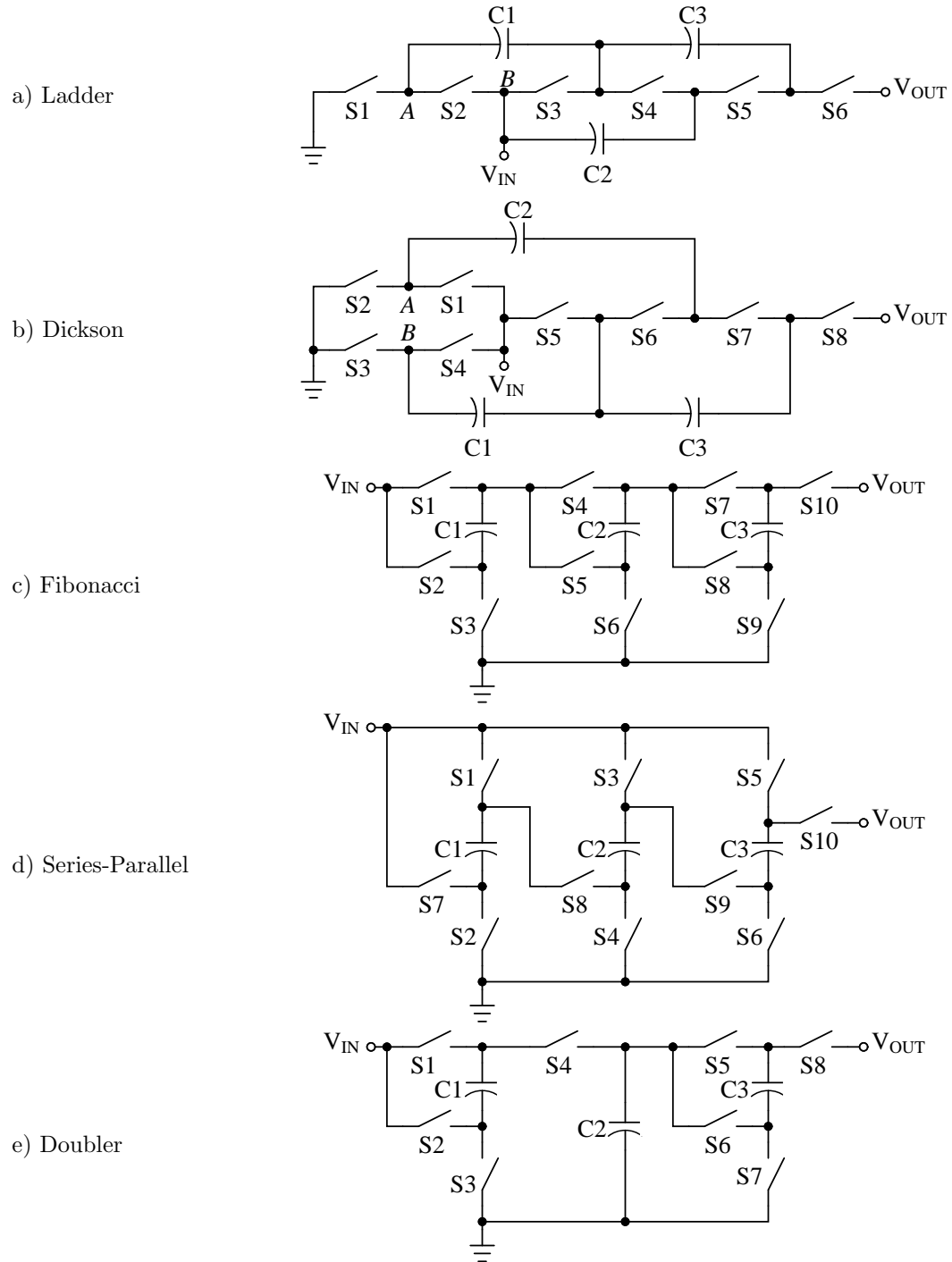


Figure 4.1. Five common switched-capacitor converter topologies in their step-up form

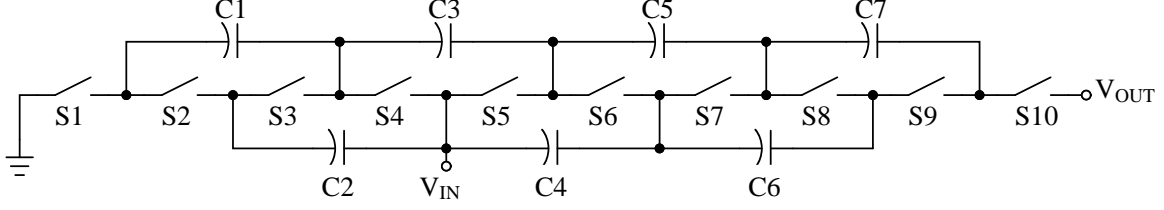


Figure 4.2. A 2:5 ladder topology

At this point, the charge multiplier for C1, the capacitor at the lowest potential with respect to ground, can be found. Since SC converters conserve charge between the input and output port constrained by their conversion ratio, in (1.1), the input charge can be found directly in terms of the output charge. If q_{out} of charge is delivered to the output during each period, then $n/m \cdot q_{out}$ of charge is pulled from the input. Since the difference between input and output charge must flow through ground by KCL, $(n/m - 1) \cdot q_{out}$ of charge must flow into ground during each period. This examination yields the charge multiplier for C1, and the remaining capacitor charge multipliers can be found by inspection:

$$|a_{c,1}| = |a_{c,2}| = (5/2 - 1). \quad (4.8)$$

In general, the first $2(m - 1)$ capacitors have charge multipliers of increasing multiples of $(n/m - 1)$, adding up to:

$$\sum_{i=1}^{2(m-1)} |a_{c,i}| = (n - m)(m - 1). \quad (4.9)$$

Similarly, the last $2(n - m) - 1$ capacitors have charge multipliers of decreasing integers, adding up to:

$$\sum_{i=2m-1}^{2n-3} |a_{c,i}| = (n - m)^2. \quad (4.10)$$

Thus, the sum of the charge multipliers for all the capacitors in the topology is given by:

$$\sum_{i \in caps} |a_{c,i}| = (n - m)(n - 1). \quad (4.11)$$

Since all capacitors block a voltage equal to the input voltage divided by m , or equivalently the nominal output voltage divided by n , the SSL converter metric for the ladder converter

can be found directly from (4.11):

$$M_{SSL} = \frac{2n^2}{(n-m)^2(n-1)^2} = \frac{2N^2}{(N-1)^2(n-1)^2} \quad (4.12)$$

where the second equality substitutes the conversion ratio N , where $N = n/m$. This SSL converter metric will be compared to that of other topologies in section 4.3.

The switch charge multipliers can be determined by looking at the charge flow through each switch with respect to the adjacent capacitor charge flow. For the switches between output (in the example in figure 4.2, switches S5 through S10), their charge multipliers are simply equal to 1. The switch charge multipliers between ground and the input (switches S1 through S4 in the example) must be found by examining the capacitors between the input and ground. By inspection, each of these switches has a charge multiplier of $|a_r| = (n/m - 1)$. Thus, the sum of the charge multipliers in the topology is given by:

$$\sum_{i \in sw} |a_{r,i}| = 2(n-m) + 2m(n/m - 1) = 4(n-m). \quad (4.13)$$

Since all switches also block a voltage equal to the input voltage divided by m , the FSL converter metric for the ladder converter can be found directly from (4.13):

$$M_{FSL} = \frac{n^2}{32(n-m)^2} = \frac{N^2}{32(N-1)^2} \quad (4.14)$$

where N is the conversion ratio (i.e. $N = n/m$). At high conversion ratios, this metric approaches an asymptote at $1/32$. This FSL converter metric will be compared to that of other topologies in section 4.3.

This topology can be modified by transforming the capacitors by placing them in parallel instead of series. In this case, each capacitor will support a higher voltage but will have a smaller charge multiplier. This transformation may be used to achieve a better fit between the topology and the devices available. For a $1 : n$ converter, if all capacitors (in each of the two ladders) are transformed such that their bottom plates share the lowest-voltage node of each ladder (nodes A and B in figure 4.1a), the total converter metric will remain the same. The device utilization of this transformed converter may improve, depending on the technology used to implement it.

4.2.2 Dickson Charge Pump

The Dickson topology [14, 66, 15], shown in figure 4.1b, improves upon the ladder topology by using two oppositely-phased flying ladders instead of a single flying ladder and a DC ladder. Similar to the ladder topology, the odd-numbered switches are turned on during phase one, and the even-numbered switches turned on during phase two. This converter is primarily useful for $1 : n$ ratios (or the step-down equivalent), so this analysis will not consider non-integer ratios. In the case where $n = 2$, the converter degenerates into a simple doubler stage, so that case will not be examined here, as it is identical to the 1:2 ladder converter.

Similar to the ladder converter, capacitor C3 (the last in the sequence) has a charge multiplier of 1. By examining the charge flow at each node during each phase, it is straightforward to determine the charge multipliers of all the capacitors. In this example, the charge multipliers are:

$$|a_{c,1}| = 2 \quad |a_{c,2}| = |a_{c,3}| = 1. \quad (4.15)$$

For a $1 : n$ converter, the charge multipliers of the $n - 1$ capacitors increase by integer steps every other capacitor. The capacitor charge multipliers follow the following sequence, starting with the capacitor closest to the input source:

$$|a_c| = \{1, 1, 2, 2, \dots\}. \quad (4.16)$$

Thus, the sum of the capacitor charge multipliers is given by:

$$\sum_{i \in caps} |a_{c,i}| = \begin{cases} \frac{n^2-1}{4} & n \text{ odd} \\ \frac{n^2}{4} & n \text{ even} \end{cases} \quad (4.17)$$

Capacitor C1 blocks the input voltage, while each of the other switches blocks twice the input voltage. The sum of the product between the charge multipliers and blocking voltages equals:

$$\sum_{i \in caps} |a_{c,i} v_{c,i}| = \frac{n^2 - n}{2}. \quad (4.18)$$

Thus, the SSL metric for the Dickson converter is given by:

$$M_{SSL} = \frac{8}{(n-1)^2} \quad (4.19)$$

This SSL converter metric will be compared to that of other topologies in section 4.3.

The switch charge multipliers can again be found by evaluating Kirchoff's Current Law (KCL) at the nodes of the topology. By inspection, switches S5 through S8 have charge multipliers equal to 1. Additionally, the charge multipliers of switches S1, S2, S3 and S4 are:

$$\begin{bmatrix} |a_{r,1}| & |a_{r,2}| & |a_{r,3}| & |a_{r,4}| \end{bmatrix} = \begin{cases} \frac{n-1}{2} & \frac{n-1}{2} & \frac{n-1}{2} & \frac{n-1}{2} & n \text{ odd} \\ \frac{n}{2} - 1 & \frac{n}{2} - 1 & \frac{n}{2} & \frac{n}{2} & n \text{ even} \end{cases} \quad (4.20)$$

The blocking voltages of switches S1 through S5, and the last switch in the chain (S8 in this example) equal the input voltage, while the other switches block twice the input voltage.

The sum of the product between the charge multipliers and blocking voltages equals:

$$\sum_{i \in sw} |a_{r,i}| v_{r,i} = 4n - 4 \quad (4.21)$$

Given this sum, the FSL converter metric can easily be computed:

$$M_{FSL} = \frac{n^2}{32(n-1)^2} \quad (4.22)$$

By inspection, we see that the FSL metric for the Dickson converter is identical to the 1 : n ladder converter. This FSL converter metric will be compared to that of other topologies in section 4.3.

This topology can be reconfigured by placing the capacitors in each ladder in parallel instead of series (i.e., placing all bottom plates of the capacitors at nodes A and B in figure 4.1b). In this case, each capacitor has a charge multiplier of 1, but increasing blocking voltages. Thus, this version of the Dickson charge pump exhibits the same FSL and SSL metrics as the series-capacitor version of the circuit, but may better match a technology. This topology is typically used to generate the programming voltage on FLASH memory chips.

4.2.3 Fibonacci Topology

The Fibonacci topology performs the highest conversion ratio for a given number of capacitors [27] of any two-phase topology. Shown in figure 4.1c, it features a string of

similar three-switch, one-capacitor cells. Each cell is phased oppositely from the one before it. In this example, the odd-numbered switches are turned on in phase one, and the even-numbered switches are turned on in phase 2.

A Fibonacci converter with k capacitors exhibits a conversion ratio of $n = F_{k+2}$, where F_{k+2} is the $k + 2^{th}$ Fibonacci number. For instance, with 3 capacitors, a conversion ratio of 5 is obtained. The j -th Fibonacci number, for $j \geq 1$ can be expressed as:

$$F_j = \frac{\phi^j - (1 - \phi)^j}{\sqrt{5}} = \{1, 1, 2, 3, 5, 8, 13, \dots\} \quad (4.23)$$

where ϕ is the golden ratio ($\phi = (1 + \sqrt{5})/2 = 1.618\dots$).

For cell j in a k -capacitor converter, counting from the left, its capacitor blocks voltage $F_{j+1} = \{1, 2, 3, \dots\}$. Similarly, by inspection, the charge multiplier of capacitor j is F_{k-j+1} . The sum of the element-based product of the charge multipliers and blocking voltages is

$$\sum_{j \in caps} |a_{c,j} v_{c,j}| = \sum_{j=1}^k F_{j+1} F_{k-j+1}. \quad (4.24)$$

No simplified form of this sum exists, so (4.24) will be used directly to find the SSL converter metric:

$$M_{SSL} = \frac{2F_{k+2}^2}{\left(\sum_{j=1}^k F_{j+1} F_{k-j+1}\right)^2} \quad (4.25)$$

The conversion ratio and converter SSL metrics are evaluated for the first eight converters, and are as follows:

$$n = \{2, 3, 5, 8, 13, 21, 34, 55\} \quad (4.26)$$

$$M_{SSL} = \{8, 2, 1.02, 0.569, 0.376, 0.262, 0.195, 0.150\} \quad (4.27)$$

The SSL metric for this converter is compared with others in section 4.3.

The switch blocking voltages and charge multipliers are found by inspection in terms of the capacitor voltages and charge multipliers. The complexity of the topology prohibits a simple closed-form solution, so they will be given in terms of a generalizable sequence. For cell j in a k -cell converter, starting from the input side, the three switches in the cell have

the following charge multipliers and blocking voltages:

$$\mathbf{a}_r(j) = \begin{bmatrix} F_{k-j+2} & F_{k-j+1} & F_{k-j+1} \end{bmatrix}^\top \quad (4.28)$$

$$\mathbf{v}_r(j) = \begin{bmatrix} F_{j+1} & F_{j+1} & F_j \end{bmatrix}^\top \quad (4.29)$$

These cell-based charge multipliers and blocking voltages can be concatenated to form the charge multiplier and voltage vectors for the converter, considering the output switch has a charge multiplier of 1 and a blocking voltage of F_k . For example, the charge multipliers and blocking voltages for the 3-cell converter in figure 4.1c are:

$$\mathbf{a}_r = \begin{bmatrix} 3 & 2 & 2 & | & 2 & 1 & 1 & | & 1 & 1 & 1 & | & 1 \end{bmatrix}^\top \quad (4.30)$$

$$\mathbf{v}_r = \begin{bmatrix} 1 & 1 & 1 & | & 2 & 2 & 1 & | & 3 & 3 & 2 & | & 2 \end{bmatrix}^\top. \quad (4.31)$$

The sum of the element-based product of the charge multipliers and blocking voltages is most easily represented as a numeric sequence computed as the product of (4.30) and (4.31):

$$\sum_i a_{r,i} v_{r,i} = \{4, 10, 24, 50, 100, 192, 360, 662, \dots\} \quad (4.32)$$

From this numeric sequence, the FSL converter metric can be easily calculated:

$$M_{FSL} = \{0.125, 0.045, 0.022, 0.0085, 0.0060, \dots\} \quad (4.33)$$

The FSL metric for this converter is compared with others in section 4.3.

4.2.4 Series-Parallel Topology

The series-parallel topology, shown in figure 4.1d, operates by first placing the capacitors in parallel with the input, charging them to the input voltage (in phase one). In phase 2, the capacitors are placed in series with the input source to transfer charge to the output. With an $(n - m) \times m$ array of capacitors, an $m : n$ ratio converter can be created (where $m < n$). Figure 4.3 shows a series-parallel 2 : 5 converter.

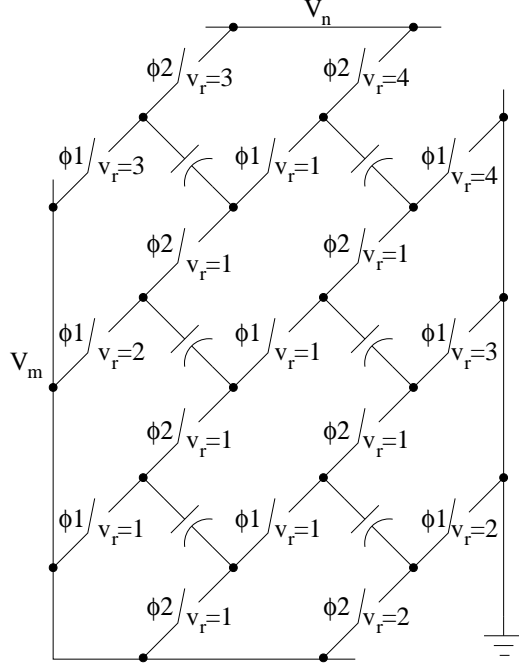


Figure 4.3. A 2:5 series-parallel topology

In phase one, the $m \cdot (n - m)$ capacitors are connected in horizontal strings of m capacitors to charge from the input source. In the second phase, the capacitors are connected in vertical strings of $n - m$ capacitors to transfer charge to the output at voltage n/m .¹ By inspection, each capacitor supports the input voltage divided by the factor m . Since m identical strings of capacitors charge the output source, each capacitor has a charge multiplier of $1/m$. Thus, the sum of the charge multiplier-voltage products can easily be found as:

$$\sum_{i \in \text{caps}} |a_{c,i} v_{c,i}| = \frac{1}{m^2} \cdot m(n - m) = \frac{n - m}{m}. \quad (4.34)$$

The SSL converter metric can be found directly from (4.34):

$$M_{SSL} = \frac{2n^2}{(n - m)^2} = \frac{2N^2}{(N - 1)^2} \quad (4.35)$$

where N is the conversion ratio of the converter, equal to the ratio of n to m . This SSL converter metric takes a simple form, and approaches an asymptote of 2 at large conversion ratios. This converter metric is compared with others in section 4.3.

¹As discussed in section A.3, this topology as posed does not guarantee capacitor voltage balancing. Additional switches must be added to make the converter well-posed, but they carry zero steady-state current and are thus neglected in this section.

A large number of switches are needed to create an $m : n$ series-parallel converter. There are $(m + 1)(n - m)$ switches that turn on in phase one, and $m(n - m + 1)$ switches that are on in phase two. By inspection, as each capacitor has a charge multiplier of $1/m$, each switch also has a charge multiplier of $1/m$. The switches not connected to one of the rails (V_m , V_n or ground) support one volt, however, some of the border switches block a higher voltage. The blocking voltages of all the switches in the 2:5 converter are indicated in figure 4.3. Through careful accounting, the sum of the switches' blocking voltages can be found:

$$\sum_{i \in sw} |v_{r,i}| = 2m(n - m) + n(n - 1). \quad (4.36)$$

Based on the uniform value of $|a_{r,i}| = 1/m$ and the voltages in (4.36), the FSL converter metric can be found:

$$M_{FSL} = \frac{n^2}{2 \left(2(n - m) + \frac{n}{m}(n - 1) \right)^2} \quad (4.37)$$

This FSL converter metric is compared with others in section 4.3.

4.2.5 Doubler Topology

The doubler topology consists of a number of 1:2 converter stages cascaded as shown in figure 4.1e. The odd-numbered capacitors (C1 and C3) are flying capacitors that shuttle charge up the ladder. The even-numbered capacitors are intermediate DC bypass capacitors. The odd-numbered switches are turned on during phase one while the even-numbered switches are turned on during phase two. For k stages (involving $2k - 1$ capacitors), the converter achieves a conversion ratio of $1 : 2^k$.

For stage j in a k -stage doubler topology, the flying capacitor blocks voltage 2^{j-1} and the DC capacitor blocks voltage 2^j . Note that the DC capacitor on the last stage is omitted. The charge multiplier of the flying capacitor in stage j is equal to $|a_{c,2j-1}| = 2^{k-j}$, while the charge multiplier of the DC capacitor is $|a_{c,2j}| = 2^{k-j-1}$. For each capacitor (flying and DC), the product between its charge multiplier and blocking voltage is equal to 2^{k-1} . Thus,

the sum of the product between the charge multipliers and the blocking voltage equals:

$$\sum_{i \in caps} |a_{c,i} v_{c,i}| = (2k - 1) 2^{k-1}. \quad (4.38)$$

The SSL converter metric can easily be found from (4.38):

$$M_{SSL} = \frac{2^{2k+1}}{(2k - 1) 2^{2(k-1)}} = \frac{8}{(2k - 1)^2} \quad (4.39)$$

where the conversion ratio $n = 2^k$. This SSL converter metric is compared with others in section 4.3. If multiple interleaved phases are used, the DC capacitors can be reduced in size, increasing efficiency. This transformation is discussed in section 4.3.1.

The switch charge multipliers and voltages can also easily be found in terms of the capacitor charge multipliers and voltages. In each stage, all four switches block the same voltage and carry the same amount of charge. Thus, for stage j in a k -stage converter, each switch blocks voltage $|v_{r,i}| = 2^{j-1}$ and has a charge multiplier of $|a_{r,i}| = 2^{k-j}$. Thus, the product of charge multiplier and blocking voltage of each switch is 2^{k-1} . Thus, the sum of the product between the charge multipliers and the blocking voltage can easily be found:

$$\sum_{i \in sw} |a_{r,i} v_{r,i}| = 4k \cdot 2^{k-1}. \quad (4.40)$$

The FSL converter metric can easily be found from (4.40):

$$M_{FSL} = \frac{2^{2k}}{32 k^2 2^{2(k-1)}} = \frac{1}{8k^2} \quad (4.41)$$

where the conversion ratio $n = 2^k$. This FSL converter metric is compared with others in section 4.3.

4.3 Comparison of SC Topologies

The SSL and FSL converter metrics for five SC topologies were calculated in section 4.2. These metrics are equal to the V-A product (or G-V² product) of each converter divided by the sum of the G-V² products of its constitutive components. Thus, the metrics are ideal for comparing the performance of different topologies, where converters with a higher

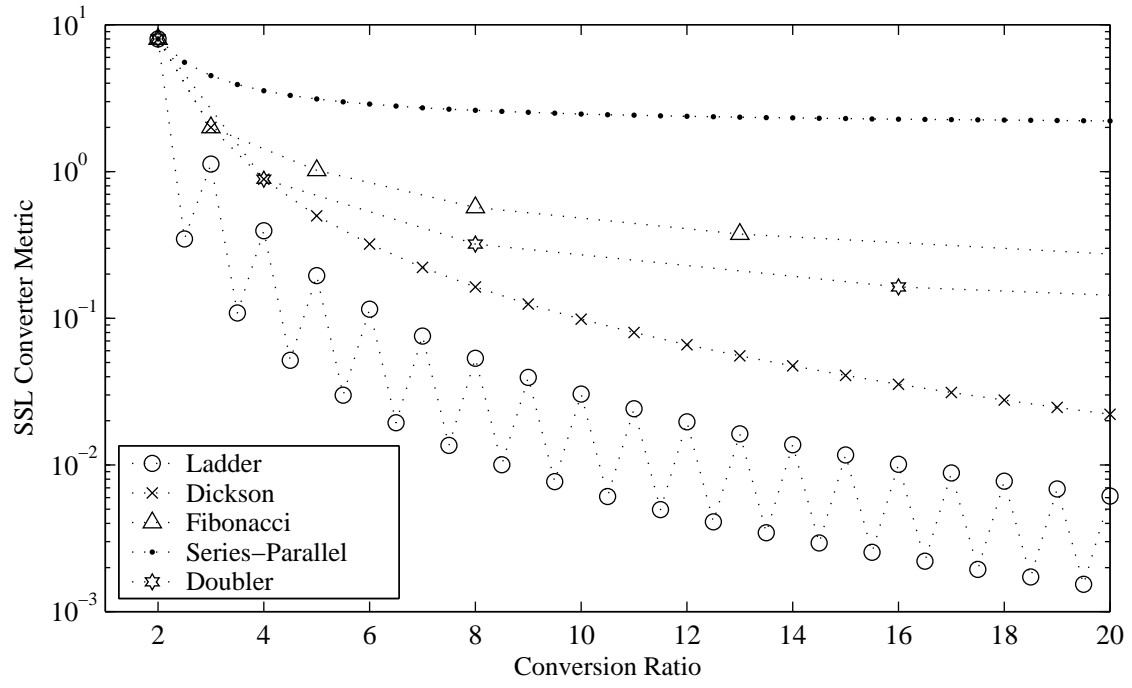
metric will perform better than ones with a lower metric. Figure 4.4 compares the SSL and FSL metrics for these five topologies on a logarithmic scale. At a 2 : 1 conversion ratio, all converters degenerate into the same single-stage doubler structure, and therefore share the same metric. At high conversion ratios, the performance of the converters differs significantly.

The ladder and series-parallel converters, analyzed for a general $m : n$ conversion ratio, are evaluated for half-integer ratios. All other topologies are evaluated for integers or the available ratios.

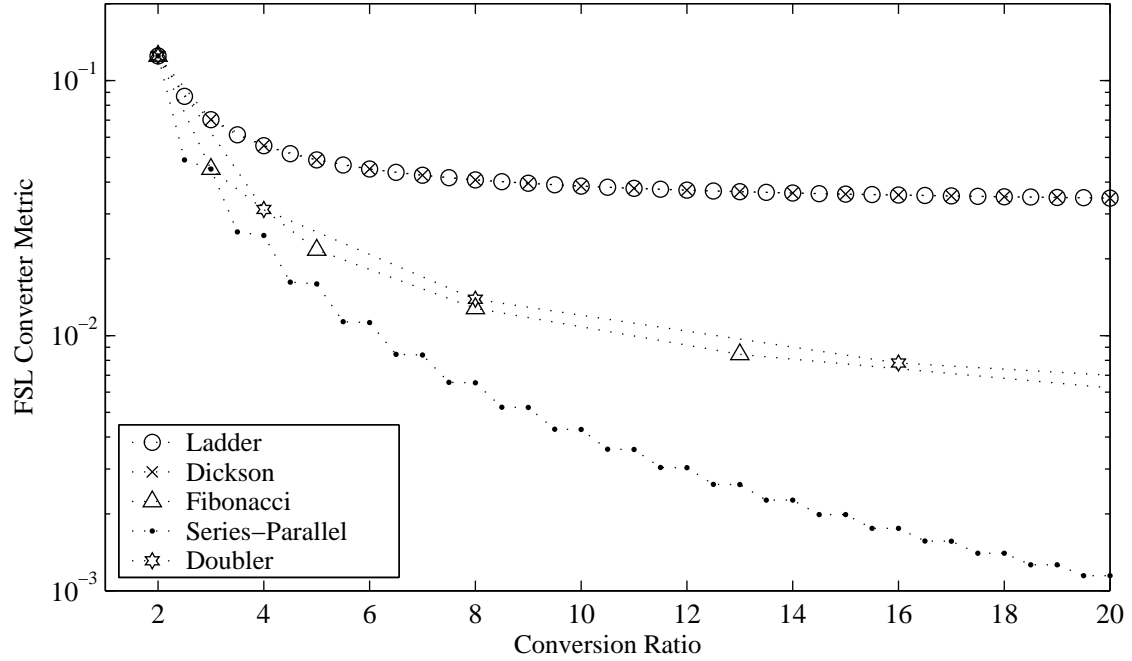
In the SSL metric comparison, shown in figure 4.4a, the series-parallel topology has the best (largest) metric of any of the five topologies. As predicted, it reaches an asymptote at 2 for large conversion ratios. The ladder topology is the worst, exhibiting an SSL converter metric 100-times lower at high conversion ratios. However, the ladder converter can be fairly efficient at small conversion ratios ($n/m \approx 1$), as seen in section 4.4.

Since the performance metrics of the series-parallel and ladder topologies were found for rational conversion ratios, it is important to consider how these topologies perform as the conversion ratio changes. The expressions for the SSL metric for the series-parallel topology in (4.35), and the FSL metric for the ladder topology in (4.14), are only dependent on the conversion ratio N , not the integer numerator n or denominator m . When considering these metrics, creating a non-integer conversion ratio does not impact efficiency with these topologies. However, the FSL metric of the series-parallel topology has a dependency on n given in (4.37). With a large denominator m , the FSL metric approaches a new limit inferior to the integer metric by a factor of up to two. Similarly, the SSL metric for the ladder topology in (4.12) has a similar dependence on the value of n , but the metric does not approach a new limit. The SSL metric for the ladder topology approaches zero as m and n increase. These properties of the series-parallel and ladder converters are important to consider when making non-integer ratio converters, such as the ladder converter in section 5.4.1.

In the FSL metric comparison, the relative performance of the five converters is nearly



(a) SSL metric (capacitor limited designs)



(b) FSL metric (switch limited designs)

Figure 4.4. Comparison of SSL and FSL converter metrics

opposite that in the SSL case. The ladder and Dickson circuit both obtain the best performance, reaching a high-conversion-ratio asymptote at $1/32$. The series-parallel topology does much worse; at a conversion ratio of 1:12, it is ten times worse than the ladder converter. The topology choice must be based on technology compatibility and the converter performance metrics for the area-limiting component type.

4.3.1 Symmetrical Topologies

The DC capacitors in the ladder and doubler topologies reduce the efficiency (and converter metrics) of those topologies by consuming die area (and contributing their charge multipliers), but do not act in shuttling charge between the input and output. The performance of these topologies can be improved by eliminating the DC capacitors. The topology can be made symmetric by using two topologies, oppositely-phased. The corresponding DC nodes on the two converters are tied together, placing the DC capacitors in parallel. Since the charge multipliers in the DC capacitors cancel each other out, the net charge multiplier through the DC capacitors is now zero. During component optimization, the size of these capacitors will be zero. Thus, their use is purely for transient absorption, and can be made much smaller.

Since only the ladder and doubler topologies have DC capacitors, only they can be transformed. Additionally, since no switches are eliminated, the FSL converter metric of the transformed converters remain unchanged. For simplicity, only the original half of the symmetrical circuit will be analyzed. For the entire topology, the number of switches and capacitors double, but each component has half the original charge multiplier. In general, by adding interleaved phases, the charge multipliers decrease as the number of components increase, so the converter metrics remain the same for topologies without DC capacitors.

The symmetric ladder topology now has $m - 1$ capacitors between the input junction and ground, with charge multipliers increasing at multiples of $n/m - 1$. Additionally, it has $n - m$ flying capacitors connecting the input to the output. For example, the charge multipliers of capacitors C1 through C4 in the 2:5 symmetric ladder topology, as shown in

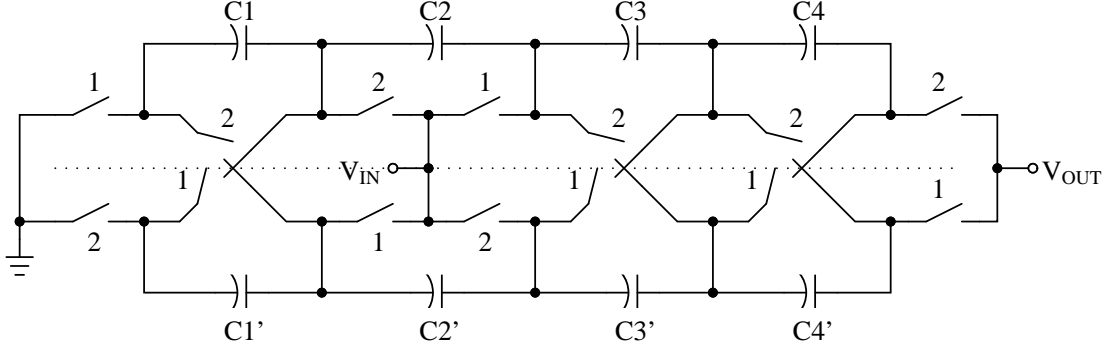


Figure 4.5. Symmetric 2:5 ladder topology

figure 4.5, are as follows:

$$|a_{c,i}| = \left\{ \begin{matrix} 3/2 & 3 & 2 & 1 \end{matrix} \right\} \quad (4.42)$$

where only the half-circuit is considered, neglecting capacitors C1' through C4'. Thus, the sum of the switch charge multipliers is given by:

$$\sum_{i \in caps} |a_{c,i}| = \frac{m}{2}(m-1)(n-m) + \frac{(1+n-m)(n-m)}{2}. \quad (4.43)$$

Since all capacitors in the ladder converter block the input voltage divided by m , the SSL converter metric is given by:

$$M_{SSL} = \frac{8n^2}{(n-m)^2(m^2-2m+n+1)^2}. \quad (4.44)$$

The symmetric doubler converter is very simple to analyze. For a k -stage converter, there are k flying capacitors (in the half-circuit), each with a product of the charge multiplier and blocking voltage equal to 2^{k-1} . Thus, the sum of the product between the charge multipliers and capacitor voltages equals:

$$\sum_{i \in caps} |a_{c,i}v_{c,i}| = k 2^{k-1}. \quad (4.45)$$

Based on the sum in (4.45), the SSL converter metric can be found:

$$M_{SSL} = \frac{8}{k^2}. \quad (4.46)$$

These metrics are significantly larger than their non-symmetric counterparts in section 4.2.

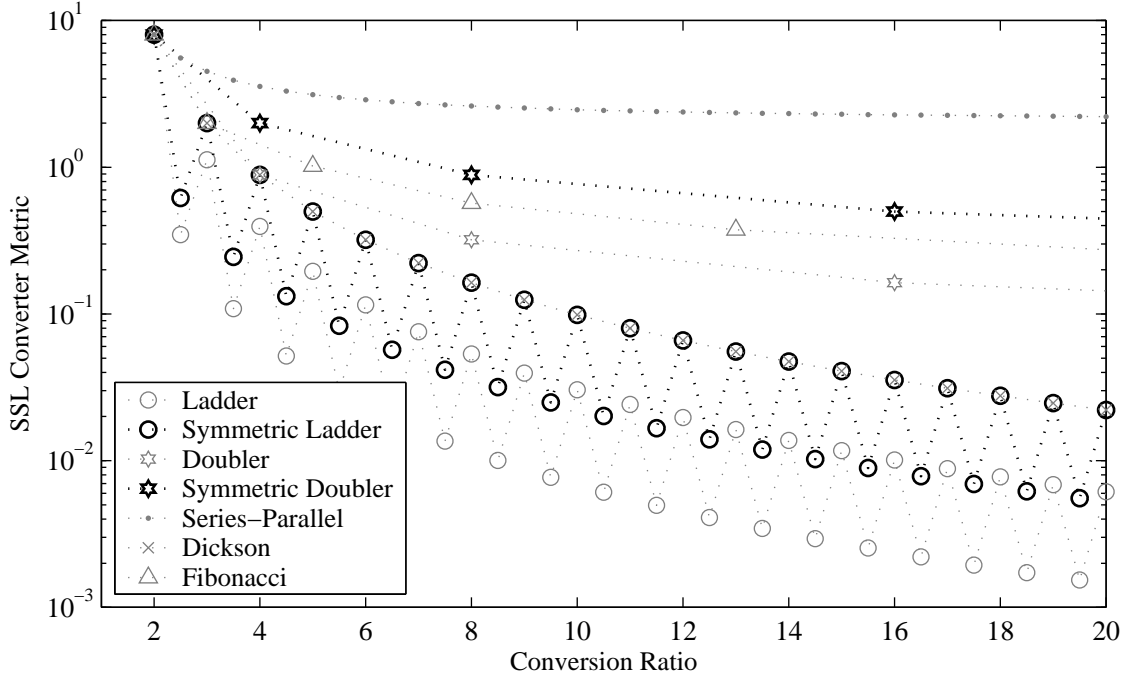


Figure 4.6. SSL metric improvement with symmetric converters

Figure 4.6 shows the SSL converter metric comparison with the symmetric ladder and doubler converter shown. The performance of these two converters is improved substantially over their non-symmetric forms. For example, the performance of the symmetric ladder equals the performance of the Dickson circuit, whereas the non-symmetric ladder topology was inferior by a factor of four at high conversion ratios. If the increase in component count is not a problem, as in an IC, using a symmetrical topology can improve efficiency.

4.4 Comparison with Magnetics-Based Converters

One of the benefits of SC converters is that they can utilize transistors and reactive elements better than traditional magnetics-based converters for many applications. In order to show how this benefit can be achieved, this section compares SC converters to two traditional magnetics-based converters. Specifically, this section examines a boost converter and a transformer-bridge converter, considering both switch and reactive-element utilization.

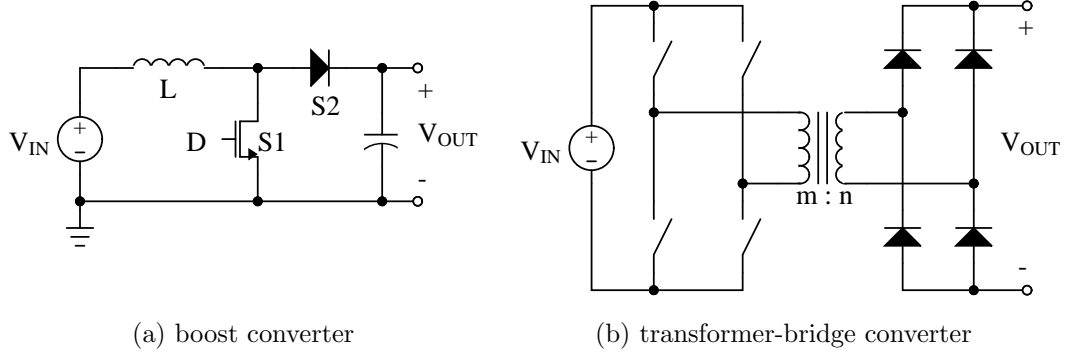


Figure 4.7. Traditional magnetics-based converters

A boost converter, shown in figure 4.7a, consists of two power switches and a single inductor. The output capacitor is used as a filter element. Also, note that the buck converter is fully equivalent to the boost converter, with differences in the polarity of current and power flow [21]. As with the switched-capacitor circuits, the output capacitor will be neglected in the analysis. The transformer-bridge converter, shown in figure 4.7b performs a fixed-ratio conversion, defined by the turns ratio of the transformer given by $m : n$. Eight switches perform the switching and rectification at an exact 50% duty cycle. Each of these two converters will be optimized for a given conversion ratio of $N = n/m$ to fairly compare with the SC converters.

4.4.1 Switch Comparison

The boost converter has a nominal conversion ratio based on the duty cycle D . The output voltage of the boost converter is given by:

$$V_{OUT} = \frac{V_{IN}}{1 - D}. \quad (4.47)$$

Thus, the conversion ratio of the circuit is simply equal to $1/(1 - D)$ in periodic steady state. To fairly compare this converter with a fixed-ratio SC converter, the boost converter will be optimized for the specific conversion ratio considered.

For this FSL analysis, strong continuous conduction will be assumed, where the inductor current I_L is nearly constant. This assumption gives the most favorable consideration of

the inductor-based converter as losses associated with ripple and inductive switching are ignored.

First, the total G - V^2 product of the switches will be constrained to X_{tot} during this optimization. Since both switches block the output voltage of the converter, a constraint is placed on the total switch conductance:

$$G_1 + G_2 = \frac{X_{tot}}{V_{OUT}^2} = (1 - D)^2 X_{tot} \quad (4.48)$$

where the input voltage is normalized to 1. The power loss due to the switch resistance can be found in terms of the switch conductances, the duty cycle and inductor current:

$$P_{SW} = I_L^2 \left(\frac{D}{G_1} + \frac{1 - D}{G_2} \right). \quad (4.49)$$

By optimizing G_1 and G_2 to minimize the switch conduction loss, the minimal loss can be found. The optimal switch conductances are proportional to the square root of their duty cycles. Thus, the optimal switch conductances are given by:

$$G_1 = \frac{\sqrt{D}}{\sqrt{D} + \sqrt{1 - D}} (1 - D)^2 X_{tot}, \quad G_2 = \frac{\sqrt{1 - D}}{\sqrt{D} + \sqrt{1 - D}} (1 - D)^2 X_{tot} \quad (4.50)$$

These conductance values can be substituted into (4.49) to find the optimized switch-based (FSL) power loss:

$$P_{SW} = \frac{1}{X_{tot}} I_L^2 \frac{(\sqrt{D} + \sqrt{1 - D})^2}{(1 - D)^2} \quad (4.51)$$

Since I_L is equal to the output current multiplied by the conversion ratio, an equivalent FSL impedance can be determined for the boost converter:

$$R_{FSL} = \frac{1}{X_{tot}} \frac{(\sqrt{D} + \sqrt{1 - D})^2}{(1 - D)^4}. \quad (4.52)$$

In terms of the conversion ratio $N = 1/(1 - D)$, the FSL impedance is:

$$R_{FSL} = \frac{1}{X_{tot}} N^3 (\sqrt{N - 1} + 1)^2. \quad (4.53)$$

The FSL converter metric can be found by substituting (4.53) into (4.2):

$$M_{FSL} = \frac{1}{N (\sqrt{N - 1} + 1)^2} \quad (4.54)$$

This FSL metric can be directly compared to the FSL converter metrics for any SC topology. This comparison is shown in figure 4.8.

The transformer-bridge converter, shown in figure 4.7b, uses eight switches at a fixed 50% duty cycle. The voltage conversion is performed explicitly by the transformer turns ratio. Thus, each switch has the same V-A product, as voltage is scaled up by the conversion ratio N and the current is scaled down by N . Without loss of generality, assume V_{IN} equals 1 volt. The input switches block 1 volt, while the output switches block N volts. Thus, the input switches have conductance $1/8$, while the output switches will have conductance $1/8N^2$ to keep the total switch G-V² equal to 1. The switch conduction loss can be found in terms of the input and output currents:

$$P_{SW} = 4 I_{IN}^2 \frac{8}{2} + 4 I_{OUT}^2 \frac{8N^2}{2} = 16 (I_{IN}^2 + N^2 I_{OUT}^2). \quad (4.55)$$

Since the input current is N times larger than the output current, the FSL loss impedance can be determined by factoring out I_{OUT}^2 :

$$R_{FSL} = 32N^2. \quad (4.56)$$

The FSL converter metric can be found by substituting (4.56) into (4.2):

$$M_{FSL} = \frac{1}{32} \quad (4.57)$$

As expected, since the voltage conversion is solely handled in the transformer, the switch-based converter metric is independent of conversion ratio.

Figure 4.8 compares the FSL (switch-based) converter metrics of the boost converter and transformer-bridge converter to the ladder and series-parallel SC topologies. The ladder converter exhibits a superior FSL metric to the other converters at all conversion ratios. At a conversion ratio of two, the boost performs equally well as both SC converters, but otherwise lags behind the ladder topology. At high conversion ratios, the boost converter is substantially inferior to either the SC ladder or transformer bridge converter. Finally the FSL metric of the ladder topology asymptotically approaches the limit of $1/32$, equal to the transformer bridge converter.

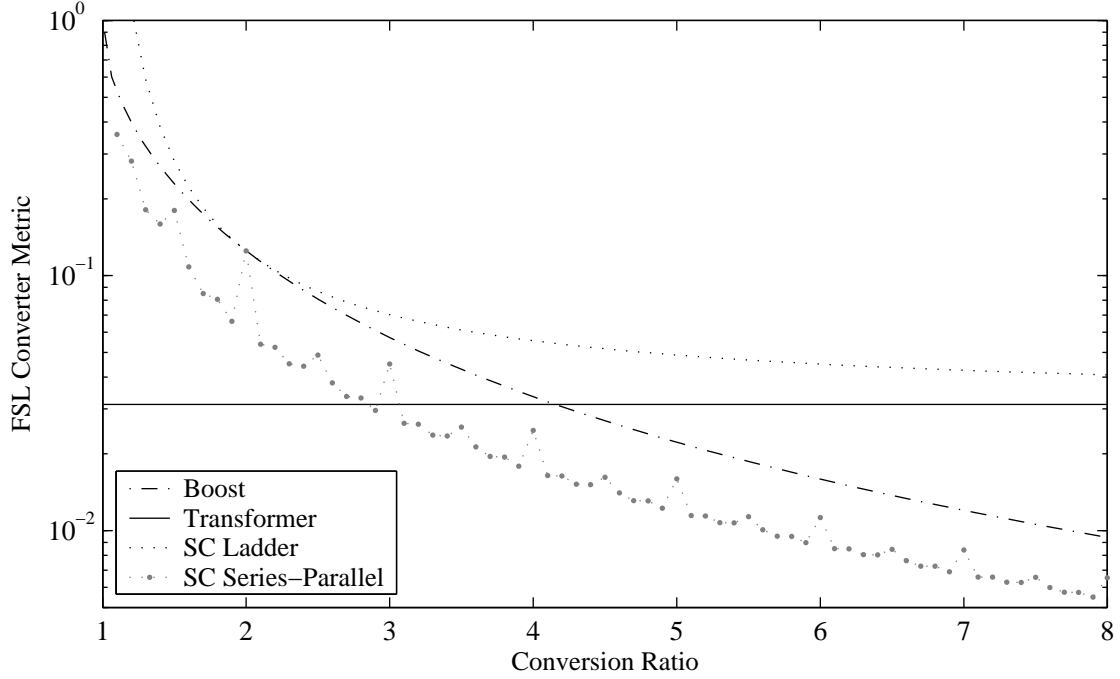


Figure 4.8. FSL metrics for magnetics-based and SC converters

At large conversion ratios, the SC ladder converter exhibits superior switch utilization compared with a traditional boost converter. At a conversion ratio of 8, the ladder converter bests the boost converter by a factor of 4. This performance difference is proportional to the conversion ratio at high conversion ratios. The total V-A product of the switches in a boost converter is proportional to the power handled by the converter and the conversion ratio N . However, the V-A product for the switches in a SC ladder approaches a fixed limit in the high-ratio asymptote. This difference allows for the superior performance of SC converters at high conversion ratios. For integer conversion ratios, the series-parallel topology is only slightly lagging with respect to the boost converter. However, the series-parallel topology can yield excellent performance due to its excellent performance when reactive elements are considered, as discussed in section 4.4.2.

4.4.2 Reactive Element Comparison

Comparing the use of reactive elements (capacitors and inductors) between SC converters and magnetics-based converters may not be straightforward, but some comparisons can be made. The SSL metric of an SC converter compares the output resistance of the converter with the energy storage of the reactive elements of that converter. Thus, for a given output power (and assumed converter efficiency), the requirements placed upon the reactive elements for the SC and magnetics-based converters will be examined. Additionally, the differences between the energy density of capacitors and inductors will be examined and incorporated into the reactance-based converter metric.

Since both the inductor in the boost converter and the transformer in the transformer-bridge converter have similar volt-second product requirements, the size of their respective magnetic components will be similar.² Additionally, inductors are more easily analyzed and examples of properly-sized inductors can be found readily. Thus, only the boost converter will be compared against SC converters.

First, the inductor energy storage requirements will be calculated. In each switching period, the inductor current ramps between two values, denoted I_{MIN} and I_{MAX} . Since the inductor current equals the input current, the average inductor current must equal the average output current multiplied by the conversion ratio, assuming that energy is conserved between the input and output of an efficient DC-DC converter. For a given conversion ratio and output power, the inductor size is minimized by being on the edge of discontinuous conduction mode (DCM), such that I_{MIN} equals zero.

When the converter is operating at the edge of DCM, the peak inductor current is equal to twice the average input current. Thus, the maximum inductor current is given by:

$$I_{MAX} = 2 I_{IN} = 2 \frac{I_{OUT}}{1 - D} \quad (4.58)$$

where D is the duty cycle of the active switch in the boost converter. The inductor current

²While the transformer for the transformer-bridge converter has nearly the same volt-second rating as the inductor for the boost converter, it does not need to store any energy, and thus may be smaller than the inductors shown here. However, most DC-DC converters need similar energy storage requirements as the boost converter, including the isolated flyback and forward converters.

ramps from zero to I_{MAX} over the first half of the switching period. Thus, the required inductance can be found in terms of the switching frequency:

$$L = V_{IN} \frac{D/f_{sw}}{I_{MAX}}. \quad (4.59)$$

By substituting (4.58) and (4.47) into (4.59), the maximum inductor energy can be found:

$$E_{L,MAX} = \frac{1}{2} L I_{MAX}^2 = \frac{1}{2} V_{OUT} \frac{D(1-D)}{f_{sw}} \left(2 \frac{I_{OUT}}{1-D} \right) \quad (4.60)$$

$$E_{L,MAX} = \frac{D}{f_{sw}} P_{OUT}. \quad (4.61)$$

Equation (4.61) represents the minimum inductor energy capacity to create a boost converter with a specific duty ratio, switching frequency and output power.

With SC converters, there is no hard relation between capacitor energy and output power. As capacitor energy is decreased, the converter's output impedance increases, yielding lower efficiency. Thus, a fixed efficiency (in terms of capacitor-based loss) will be assumed. In this example, an efficiency of 95% will be assumed, as that likely reflects the switch losses of a boost converter designed on the edge of DCM.

Since the output voltage of the converter drops with the output resistance, the efficiency of an SC converter is given by:

$$\eta = \frac{n V_{IN} - I_{OUT} R_{OUT}}{n V_{IN}} \quad (4.62)$$

when considering only the SSL power loss. Thus, the required output impedance for a certain efficiency η is given by:

$$R_{OUT} = (1 - \eta) \frac{n V_{IN}}{I_{OUT}} \quad (4.63)$$

The energy storage for a given SC topology to obtain a certain efficiency can be found by substituting (4.63) into (4.1) and solving for E_{TOT} :

$$E_{tot} = \frac{2 V_{OUT}^2 / R_{SSL}}{f_{sw} M_{SSL}} = \frac{2 P_{OUT}}{(1 - \eta) f_{sw} M_{SSL}}. \quad (4.64)$$

Type	Manufacturer	Capacitance	Dimensions	Energy Density
			WxLxH [mm ³]	[μJ/mm ³]
Ceramic	Taiyo-Yuden	22 μF @ 4V	1.6x0.8x0.8 (0603)	344
	Taiyo-Yuden	1 μF @ 35V	1.6x0.8x0.8 (0603)	1196
Tantalum	Vishay	10 μF @ 4V	1.0x0.5x0.6	533
	Vishay	100 μF @ 6.3V	2.4x1.45x1.1	1037
Electrolytic	Kemet	100 μF @ 6.3V	7.3x4.3x2.8	45
	Kemet	22 μF @ 16V	7.3x4.3x1.9	94
	C.D.E.	210 mF @ 50V	76φx219	172

(a)

Type	Manufacturer	Inductance	Dimensions	Energy Density
			WxLxH [mm ³]	[μJ/mm ³]
Shielded SMT	Coilcraft	10 μH @ 0.21 A	2.6x2.1x1.8	0.045
Shielded SMT	Coilcraft	100 μH @ 0.10 A	3.4x3.0x2.0	0.049
Shielded	Coilcraft	170 μH @ 1.0A	11x11x9.5	0.148
Shielded	Murata	1 mH @ 2.4A	29.8φx21.8	0.189

(b)

Table 4.1. Energy densities of common (a) capacitors and (b) inductors

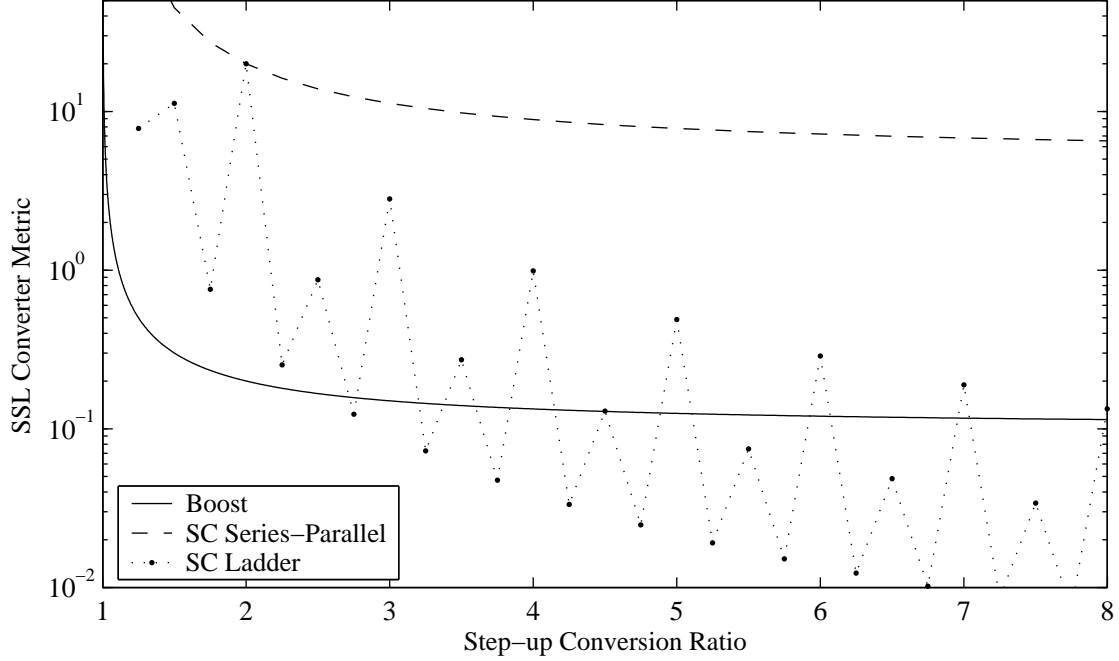


Figure 4.9. SSL metrics for magnetics-based and SC converters

Equation (4.64) represents the total capacitor energy to obtain a given (SSL-loss-based) efficiency for a given topology.

However, the comparison between inductor energy storage and capacitor energy storage must consider the energy density of the particular energy storage devices. Since power inductors cannot be practically implemented on-die, a comparison between the energy storage of discrete capacitors and inductors will be used. Table 4.1 lists the energy density for a number of readily available capacitors and inductors. By inspection, the volumetric energy density of capacitors exceeds the energy density of inductors by over a thousand times. The following comparison will assume a capacitor volumetric energy density of $100 \mu\text{J}/\text{mm}^3$ and a inductor volumetric energy density of $0.1 \mu\text{J}/\text{mm}^3$.

Based on the reactance energy storage requirement derived in this section and the SSL converter metrics derived in section 4.2, the output power of a converter can be compared to the volume of its reactive element(s). The boost converter is compared to SC ladder and series-parallel topologies in figure 4.9. An efficiency of 95% was assumed for the SC

converters. The performance of the SC series-parallel topology exceeds the power density of the boost converter by nearly fifty times for a given conversion ratio and physical reactance volume, due to the significant difference in energy density between capacitors and inductors.

The SC series-parallel topology is an excellent candidate for IC integration as it exhibits superior capacitor utilization and adequate switch utilization, as shown in figure 4.8. Both the series-parallel and ladder topologies are advantageous to magnetics-based converters at moderate conversion ratios. The two comparisons performed in this chapter conclude that an appropriately-designed switched-capacitor converter can have a higher power density than a traditional magnetics-based DC-DC converter.

4.5 Fundamental Performance Limits

The performance of a number of SC power converters has been compared in both the SSL and FSL in section 4.3. Additionally, several SC converters were compared with a traditional boost converter and transformer-bridge converter. It was found that a SC topology performed superiorly to the traditional magnetics-based converters across a range of conversion ratios. These comparisons raise the question whether a fundamental maximum exists for the performance metrics of SC converters. Based on the network analysis methods developed by Wolaver in references [60, 61], we can derive a fundamental limit on both the SSL and FSL converter metrics in terms of the conversion ratio.

A few terms used in the derivation [60, 61] must be first explained. In steady-state converter operation, each component dissipates an *average power* \overline{P} , composed of an *ac power* P_{ac} and a *dc power* P_{DC} . These properties apply to any circuit, not just SC converters. The average power dissipated by an element is given by:

$$\overline{P} = \overline{v i} \tag{4.65}$$

where v and i are the instantaneous voltage across and current through the element, respectively, and the over-line represents the time-average of the quantity underneath the line. This average power can be broken down into two components, *dc power* and *ac power*,

where the *dc power* is given by the product of average voltage and average current:

$$P_{dc} = \bar{v} \bar{i} \quad (4.66)$$

and the *ac power* is simply given by the remainder:

$$P_{ac} = \bar{P} - P_{dc} = \overline{(v - \bar{v})(i - \bar{i})}. \quad (4.67)$$

Switches in a DC-DC converter, with very low on-state resistance and near-infinite off-state resistance, have nearly zero average power. Switch power loss is a parasitic effect in these circuits. For diodes (and other passive switches), which conduct a negative current with respect to the voltage they block, have negative *dc power* and positive *ac power*. They are designated *dc active* since they absorb negative *dc power*. Controlled switches, conducting a positive current while on and blocking positive voltage while off, have positive *dc power* (and thus negative *ac power*). These switches are designated as *ac active*, because they absorb negative *ac power*.

4.5.1 SSL Converter Metric Limit

In order to find a limit on the SSL converter metric, a relationship between the conversion ratio and output power of the circuit and the reactances must be used. Wolaver [60, 61] states and proves the following relation:

$$\frac{1}{2} \sum_{k \in caps} \overline{|v_k i_k|} \geq \frac{N-1}{N} \overline{P_{OUT}} \quad (4.68)$$

where N is the current or voltage step-up ratio (whichever is greater than one), and v_k and i_k are the instantaneous voltage across and current through capacitor k . For an inductor-based converter, this relation applies over all reactances in the circuit.

The SSL converter performance metric in section 4.1 considers low-load conditions where the capacitor voltages equal their no-load steady-state voltages. The capacitor voltages will be defined such that they are all positive. In this analysis, the switch voltage drops and voltage ripple on the capacitors will also be neglected. Thus, the capacitor voltages in (4.68)

will be assumed constant, yielding:

$$\frac{1}{2} \sum_{k \in caps} v_k \overline{|i_k|} \geq \frac{N-1}{N} V_{OUT} I_{OUT}. \quad (4.69)$$

In periodic steady-state, the time-averaged capacitor current is given as the sum of the charge flows in the capacitor over each clock phase j , multiplied by the switching frequency:

$$\overline{|i_k|} = \sum_{j=1}^n \left| a_{c,k}^j \right| q_{out} f_{sw} = \sum_{j=1}^n \left| a_{c,k}^j \right| I_{OUT}. \quad (4.70)$$

Substituting (4.70) into (4.69) yields a constraint for the capacitor parameters:

$$\sum_{k \in caps} v_{c,k} \sum_{j=1}^n \left| a_{c,k}^j \right| \geq \frac{2(N-1)}{N} V_{OUT}. \quad (4.71)$$

To substitute (4.71) into the SSL converter metric, this sum must be further transformed. A known relationship [10] between l_1 and l_2 norms can be applied to the sum of the squares of the charge multiplier vector:

$$\sum_{j=1}^n \left(a_{c,i}^j \right)^2 \leq \left(\sum_{j=1}^n \left| a_{c,i}^j \right| \right)^2 \leq n \sum_{j=1}^n \left(a_{c,i}^j \right)^2. \quad (4.72)$$

Substituting the second inequality in (4.72) into (4.71) yields:

$$\sum_{k \in caps} v_{c,k} \sqrt{n \sum_{j=1}^n \left(a_{c,k}^j \right)^2} \geq \frac{2(N-1)}{N} V_{OUT}. \quad (4.73)$$

After this substitution, (4.73) can be substituted into (4.5) to find a limit on the SSL converter metric, given by:

$$M_{SSL} \leq \frac{n N^2}{(N-1)^2}. \quad (4.74)$$

where n is the number of phases in the converter and N is the (step-up) conversion ratio.

Through the application of Wolaver's analysis of dc-dc converters based on graph theory, a limit on the SSL converter metric of a SC converter can quickly be obtained. This maximum limit, by inspection, equals the SSL converter metric for the series-parallel topology for any given rational conversion ratio. Thus, the series-parallel circuit achieves the highest performance (in the SSL) for a given amount of capacitance of any two-phase SC topology.

4.5.2 FSL Converter Metric Limit

The fundamental limit on the FSL converter metric can be found via a similar method to the SSL converter metric limit found in section 4.5.1. Since this analysis considers DC-DC converters using ideal resistive switches, it holds for all SC and magnetics-based DC-DC converters. Because the FSL converter metric examines low-load conditions, the voltage drop across on-state switches is neglected. Thus, the average power absorbed (or dissipated) by these switches is zero. If $v_{r,i}^j$ is denoted as the blocking voltage of switch i during phase j , then $v_{r,i}^j \cdot a_{r,i}^j = 0$ for all i and j .

As previously introduced, the switches in any SC converter can be divided into two disjoint sets: the *dc-active* set, made up of *dc-active* switches, and the *ac-active* set, made up of *ac-active* switches. Wolaver [60, 61] states and proves the following relation:

$$- \sum_{i \in R_{dc}} P_{dc,i} \geq \frac{N-1}{N} \overline{P_{OUT}} \quad (4.75)$$

where R_{dc} is the set of *dc-active* switches and N is the current or voltage step-up ratio of the converter (whichever is greater than one). A corollary of (4.75) is:

$$- \sum_{i \in R_{ac}} P_{ac,i} \geq \frac{N-1}{N} \overline{P_{OUT}} \quad (4.76)$$

where R_{ac} is the set of *ac-active* switches and $P_{ac,i}$ is the *ac power* absorbed by switch i .

In this analysis, equal duty cycles will be assumed such that each sub-period has duration T/n , where n is the number of phases. The *dc power* absorbed by switch i can be written as:

$$P_{dc,i} = \overline{v_{r,i}} \overline{i_{r,i}} = \frac{1}{n} I_{OUT} \sum_{j=1}^n v_{r,i}^j \sum_{j=1}^n a_{r,i}^j \quad (4.77)$$

where $v_{r,i}^j$ and $a_{r,i}^j$ are the blocking voltage and charge multiplier of switch i in clock phase j , respectively. Since the average power of a switch is zero, the *ac power* dissipated by a switch is obtained by simply negating the *dc power*. Since *dc-active* switches absorb negative *dc power* and *ac-active* switches absorb negative *ac power*, (4.66) and (4.67) can be substituted into (4.75) and (4.76), respectively. Adding the two resulting equations yields a limit on

the sum of the products between the blocking voltages and charge multipliers:

$$\frac{1}{n} I_{OUT} \sum_{i \in sw} \left[\sum_{j=1}^n v_{r,i}^j \sum_{j=1}^n |a_{r,i}^j| \right] \geq 2 \frac{N-1}{N} P_{OUT}. \quad (4.78)$$

To further simplify (4.78), the number of phases each switch is on must be known. Let k_i be the number of phases that switch i is on, where $1 \leq k_i \leq n-1$. With this definition, and the inequality in (4.72), (4.78) can be simplified to:

$$\sum_{i \in sw} \frac{n-k_i}{n} v_{r,i} \sqrt{k_i \sum_{j=1}^n (a_{r,i}^j)^2} \geq 2 \frac{N-1}{N} V_{OUT}. \quad (4.79)$$

To find the maximum metric, k_i must be chosen to minimize the sum. Let k^* be the optimal number of phases (out of n) that each switch is on, which will be optimized later. Equation (4.79) can then be simplified to:

$$\sum_{i \in sw} v_{r,i} \sqrt{\sum_{j=1}^n (a_{r,i}^j)^2} \geq 2 \frac{n}{(n-k^*) \sqrt{k^*}} \frac{N-1}{N} V_{OUT}. \quad (4.80)$$

Equation (4.80) can be substituted into (4.4) to find the fundamental FSL converter metric limit:

$$M_{FSL} \leq \frac{k^* (n-k^*)^2}{4 n^3} \frac{N^2}{(N-1)^2} \quad (4.81)$$

where n is the number of phases, k^* is the optimal duty cycle (number of phases for which each switch is on), and N is the step-up conversion ratio. For a general multiphase converter, k^* should be optimized to maximize this limit. By performing this optimization, the optimal value of k^* is found to equal $n/3$, where n is the number of clock phases. If this value is substituted into (4.81), the resulting limit equals:

$$M_{FSL} \leq \frac{1}{27 n} \frac{N^2}{(N-1)^2} \quad (4.82)$$

where n is the number of phases in the converter and N is the step-up conversion ratio.

For two-phase converters, $k^* = 1$ by necessity, as every switch is on during one phase and off during the other. Thus, (4.81) can be simplified for two-phase converters:

$$M_{FSL} \leq \frac{N^2}{32 (N-1)^2}. \quad (4.83)$$

This limit for the FSL converter metric sets a fundamental limit of converter performance. The FSL converter metric for the ladder topology is equal to this fundamental limit for two-phase converters. Thus, the ladder topology and its variations utilize switches better than any other two-phase topology. These fundamental limits can be applied as well to all DC-DC converters, showing that no magnetics-based converters could have a higher FSL metric than the ladder-based SC converter.

Chapter 5

Regulation of Switched-Capacitor Converters

While switched-capacitor (SC) DC-DC converters transform voltages at fixed conversion ratios, many applications require output regulation to deliver a constant output voltage against variations in line voltage and load current. Output regulation is necessary for sensitive loads, such as sensors or radios, where small changes in output voltage can affect functionality. Additionally, by maintaining a constant output voltage, the supply rail of the load can be maintained at the minimum tolerable voltage, minimizing current consumption. In energy-harvested or battery-operated devices, minimizing current consumption by maintaining a low but constant voltage rail can improve device lifetime significantly. Finally, in some applications, where CMOS devices are operated close to their rated voltage, voltage regulation is required to ensure the devices are not over-stressed with variation in line voltage.

Unlike inductor-based converters, where the conversion ratio is arbitrarily set by duty cycle, SC converters exhibit one (or several) conversion ratios. Further regulation is performed by modulating the output resistance of the converter in response to changing line

voltage or load current vary. The output of an SC converter is given by:

$$V_{OUT} = n V_{IN} - i_{OUT} R_{OUT}(f_{sw}, D_i G_i). \quad (5.1)$$

Equation (5.1) shows four variables that can be used to control the output voltage of an SC converter. First, the conversion ratio n is a function of topology, but can be chosen from a discrete set for variable-ratio converters, as described in section 5.4. The remaining three variables, switching frequency f_{sw} , switch duty cycle D_i and switch conductance G_i , affect the output resistance of the converter.

By changing the converter's output resistance, the output voltage of the converter will vary with the product between output current and resistance. Regulation by varying output resistance is lossy, as power is dissipated to create this voltage drop. At first look, this method of regulation is equivalent to using a linear low-dropout regulator (LDO), however, no additional power components are used and switching losses can be reduced. Additionally, by modulating output resistance, the converter becomes much more sensitive to quick changes in load, and the converter's controller must be sufficiently fast to handle these transients.

Since the load range of a SC converter often varies over many orders of magnitude, the output resistance must also be modulated over many orders of magnitude in order to effect voltage regulation. Out of the three variables affecting output resistance (f_{sw} , D_i and G_i), only switching frequency can be easily varied over the necessary range. Thus, in the regulation schemes discussed in this chapter, switching frequency will be the primary adjustment.

Figure 5.1 shows the efficiency of a 2:1 ratio converter using three control schemes. The converter is optimized for operation at 1 amp (denoted by the star). When running the converter open loop, fixing the switching frequency and switch size at the design point, the output voltage is unregulated and efficiency decreases quickly at low power levels. Using simple frequency modulation (shown by the solid curve), output regulation is performed while varying frequency roughly proportional to output power. By keeping transistor switching loss, discussed in section 3.3.1, proportional to output power, efficiency is held nearly con-

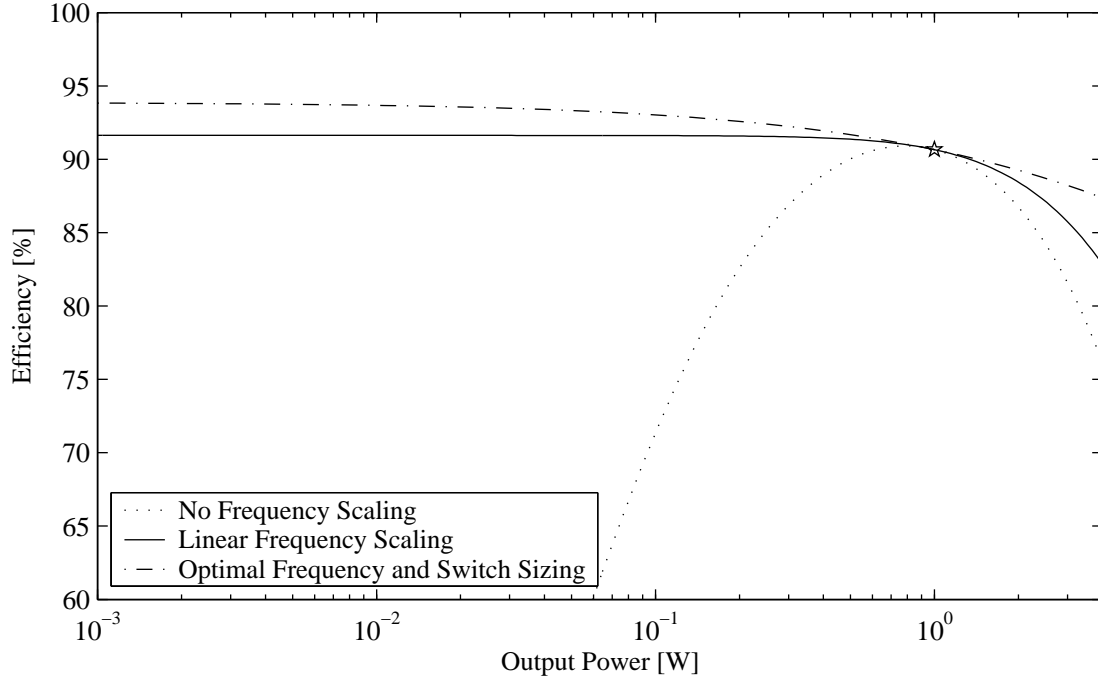


Figure 5.1. Efficiency during power backoff; 2:1 converter

stant across the range of power levels. Since switch conductance losses are reduced by the square of output current, efficiency at low power level is increased slightly over the efficiency at the design point.

By dynamically adjusting both switch size and switching frequency as output power varies, the optimal design at all power levels can be obtained. At low power levels, efficiency increases dramatically, only limited by the capacitor bottom-plate parasitic. This control method, if practical, promises a high efficiency at power levels below the design point. Additionally, varying switch size has other advantages, such as output ripple control, as discussed in section 5.1.

5.1 Output Ripple of Multiphase Converters

The ripple at the output of an SC converter can affect both the performance of the converter and the operation of the load. Many analog and digital loads are very sensitive

to ripple or noise on the supply rail, so the converters supplying these loads must reduce ripple as much as possible. However, integrated switched-capacitor converters are infamous for their large ripple voltage levels [6]. This section will examine the effects of using an SC converter with multiple interleaved phases on the output voltage ripple.

Output ripple in an SC converter is attributable to the impulse-like charge transfer in SSL operation. While the analysis in chapter 2 used a voltage-source load, real converters typically have resistive loads (or current-source-like loads) with an output capacitor. The output capacitor filters the impulses of charge from the SC converter while supplying a near-constant current to the load. In the worst case, where a step-up converter delivers charge to the load once per period, and is operating solely in the SSL, the converter’s peak-to-peak output voltage ripple would equal:

$$V_R = \frac{I_{OUT}}{f_{sw} C_{OUT}}. \quad (5.2)$$

Since the switching frequency of a converter is roughly proportional to the output current, the output ripple amplitude will remain constant over a wide range of power levels, and is simply related to the converter design and output capacitance.

Since practical ripple requirements dictate that the output capacitor must be large for many applications, it adds significantly to the die or board area requirement of the converter. For many applications, the required output capacitance would dominate the flying capacitors. Methods of reducing the size of this capacitor are necessary for on-die converters [6].

This section examines using multiple interleaved phases to reduce the ripple voltage without increasing the size of the output capacitor. Just like high-performance inductor-based converters, using interleaved phases reduces the output ripple for a given switching frequency. In an SC converter using N interleaved phases, the topology used is replicated N times and each component linearly scaled by $1/N$ in size. The clock feeding each of the interleaved phases is offset by an angle of $360^\circ/N$. In SSL operation, by having N interleaved phases, the output ripple is reduced by a factor of N . A practical limit to the number of interleaved phases used arises when the control and gate-drive power of each

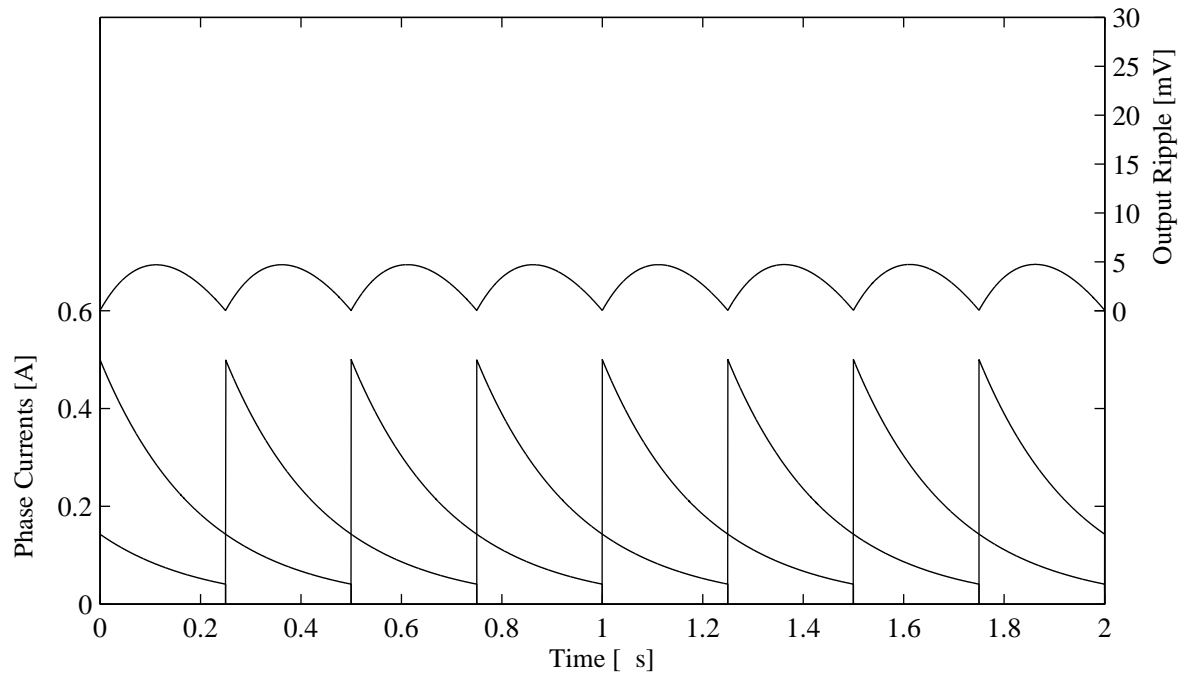
interleaved phase becomes a significant component to the power loss, negatively impacting efficiency. Section 8.2.2 discusses the optimal sizing of an individual interleaved phase cell.

At the maximum switching frequency and load, the converter is usually designed to operate in the region between the SSL and FSL, based on the optimization in section 3.3. In the operating region between the SSL and FSL, the currents flow in exponentially-decaying patterns instead of impulses. When multiple interleaved phases are used in this operating region, the current pulses overlap, greatly reducing the amplitude of the ripple voltage at the output. To illustrate this effect, the ripple voltage will be computed for an N -interleaved-phase converter over a range of switching frequencies.

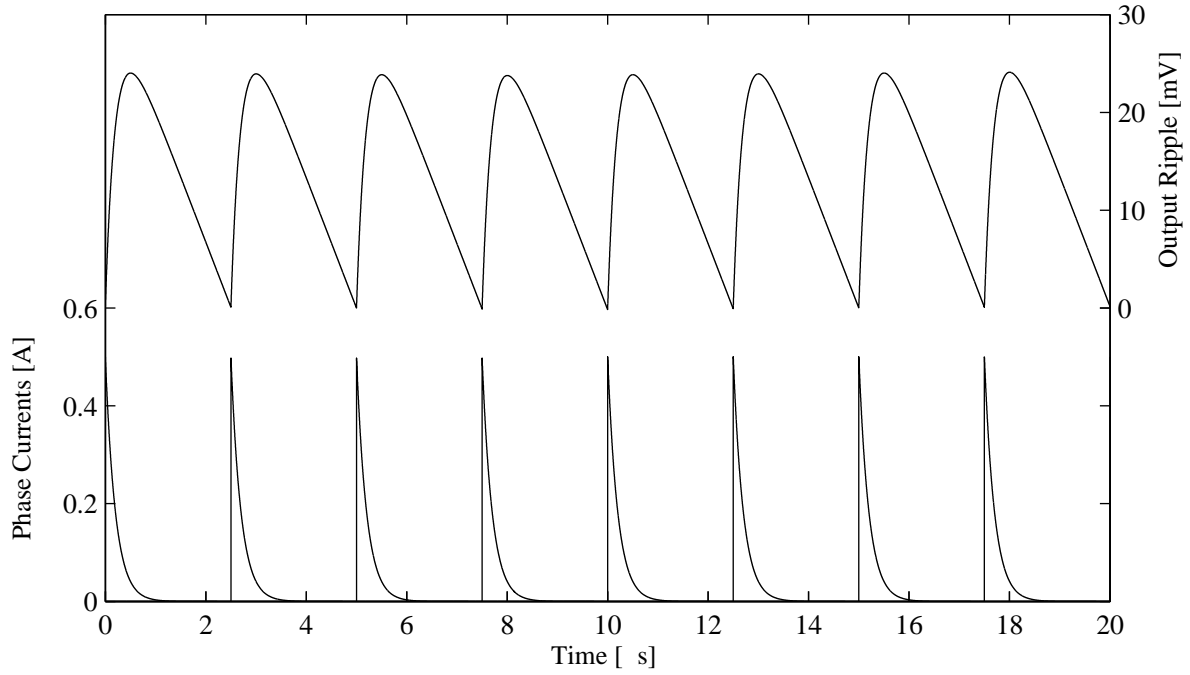
In examining the ripple voltage of an SC converter, a simple 2:1 step-down converter with four interleaved phases is considered. Each interleaved phase is an instantiation of the 2:1 converter each phased 90 degrees apart. In each interleaved phase, each of the four switches has an on-state resistance of R_{ON} and the single flying capacitor has capacitance C . Thus, during each phase transition, an exponentially-decaying pulse of charge is transferred from the input to the output. The time constant τ of this decay is equal to $2 R_{ON} C$, as the capacitor charges and discharges through two series switches.

Figure 5.2 shows the output voltage ripple and the current delivered to the output of the converter in each of the four interleaved phases. In the full-load case where the switching period is on the order of the RC time constant, the interleaved current pulses average to a low-amplitude output current, thus dramatically reducing the output ripple. At lower output loads and switching frequencies (in figure 5.2b), the currents in the four phases are nearly impulsive, allowing the full SSL ripple voltage (in (5.2)) to occur at the output.

Figure 5.3 shows the output voltage ripple of the 2:1 converter as the output power changes using either two, four or eight interleaved phases. In this example, the output voltage is regulated at a constant 0.9 V for a 2 V input by controlling the switching frequency. At full load (near 1A), the switching frequency is sufficiently fast, compared to the time constant $\tau = 2R_{ON}C$, that the ripple is only a few millivolts. At lower power levels, the ripple voltage reaches an asymptote of approximately 25 mV with four interleaved phases,



(a) Full load, $T = 1 \mu s$



(b) One-tenth load, $T = 10 \mu s$

Figure 5.2. Current transfer and output voltage ripple waveforms of a regulated four-phase 2:1 converter

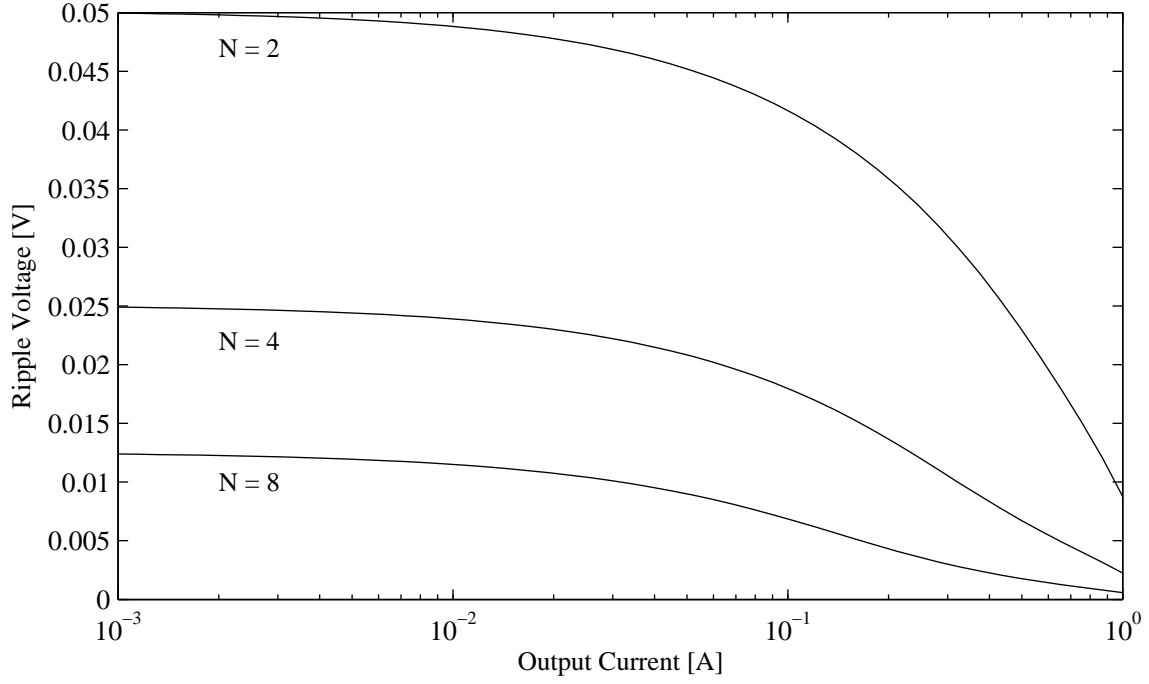


Figure 5.3. Output voltage ripple of an N -interleaved-phase 2:1 converter

set by (5.2). At full load, the output voltage ripple can actually be reduced by a factor of the square of the number of interleaved phases, as the currents in each phase combine.

The output voltage ripple of an SC converter has been examined in terms of the number of interleaved phases and the switching frequency. The use of multiple interleaved phases reduces the size of each charge pulse and reduces the output ripple in the SSL by a factor of N , where N is the number of interleaved phases. Additionally, near the maximum switching frequency, the converter operation point leaves the SSL, and the output voltage ripple can be empirically reduced by a factor of N^2 . In this region, the converter currents are no longer impulses but instead decaying exponentials in each period. As current is delivered to the output capacitor more uniformly, output voltage ripple is reduced. Using multiple interleaved phases can reduce the ripple at the output of an integrated SC converter.

5.2 Hysteretic Feedback Methods

A traditional control method for an SC converter may include a linear compensator and a voltage-controlled oscillator (VCO). However, obtaining stability and good transient response over varying load conditions using such a control method is difficult and requires sensing of the output current, as described in section 5.3. The simplest voltage regulation method for SC converters uses hysteresis for frequency control instead of a control method based on a smooth compensator. Two methods for hysteretic control will be presented, the traditional hysteretic feedback scheme, using upper and lower hysteretic bounds, and a novel lower-bound control method. Both methods use voltage references and comparators to create and detect the voltage limits, and then change the state of the converter. By eliminating filters in the converter control, the quiescent current of the controller can be dramatically reduced. Additionally, as the controller has no analog state, the converter can react to very fast loading and unloading transients.

The PicoCube power conversion IC, as described in chapter 7, utilizes a double-bound hysteretic control scheme. A block diagram of this control scheme is shown in figure 7.12. This converter uses small (approximately 1 nF) internal capacitors with a larger external capacitor (1 μ F). Thus, the inherent ripple voltage at the output is negligible. An internally-generated reference voltage is used to create two hysteresis bounds, separated by approximately 20 mV for the 2.1V rail, and 10 mV for the 0.7 V rail. When the output voltage reaches the upper limit, the converter clock (about 30 MHz) shuts off, and the output capacitor is discharged by the load current. When the output voltage dips below the lower threshold, the converter is enabled again, charging the output capacitor. Assuming the load current remains below the current delivered to the output at maximum switching frequency and minimum voltage levels, the output voltage will be held between the two hysteresis limits.

Figure 5.4 shows a load transient for the PicoCube power conversion IC from experimental data. To the left and right of the transient, the converter runs controlled, where the output is (roughly) constrained within the hysteresis bounds. Since the PicoCube IC

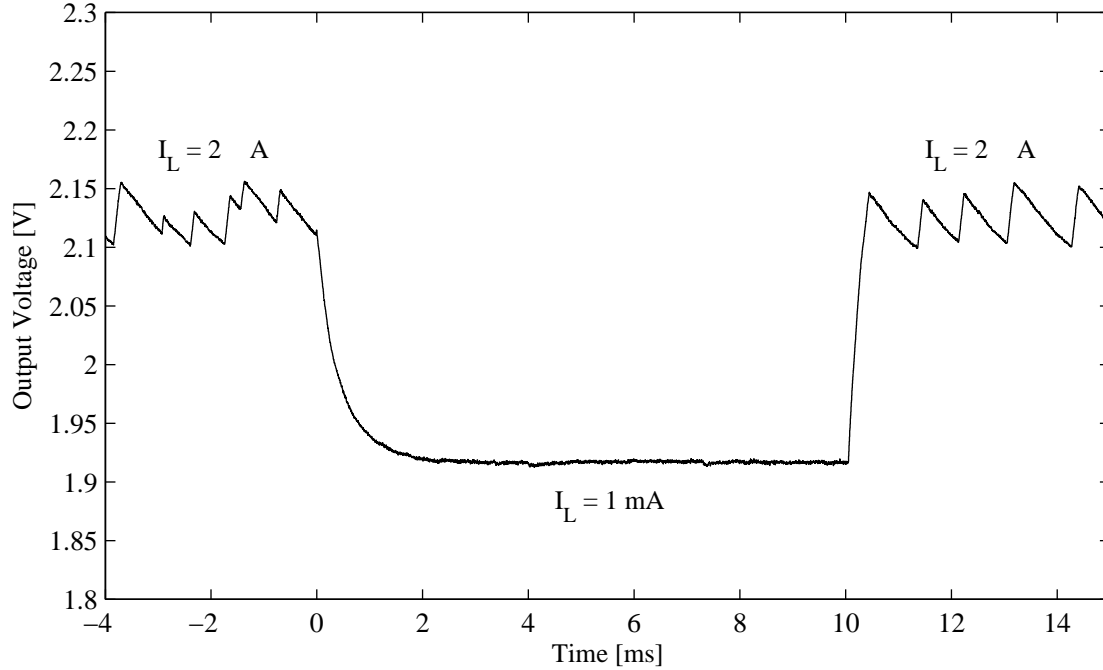


Figure 5.4. Double-bound hysteresis feedback for the PicoCube application

uses sampled comparators instead of continuous-time comparators, the hysteretic bound transitions are delayed to the next clock cycle before the clock changes mode. Thus, the exact levels of the output transitions are irregular and the ripple magnitude can exceed the set hysteretic bounds.

In the center of the waveform, the load current exceeds what the converter can deliver at full load at the lower hysteresis bound. The output voltage falls below the threshold, and the converter operates at the full switching frequency of 30 MHz until the load is reduced. This operating condition represents an unusual condition when either the load current exceeds the design point or the input voltage falls below the minimum limit. In the latter case, this operating condition can be detrimental to battery lifetime as excess gate power is consumed. A low-voltage protection circuit should be added to any system using this type of control to prevent a rechargeable battery from being destroyed in this condition.

In converters where the output capacitance is on the same order of magnitude as the

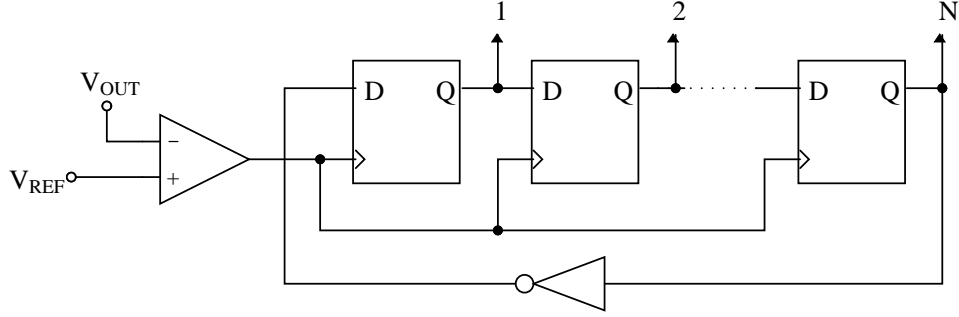


Figure 5.5. Lower-bound hysteretic feedback controller

flying capacitors, the output ripple can be significant. This ripple can be used directly to control the converter. During each phase transition in an interleaved phase, a packet of charge is delivered to the output.¹ This charge packet raises the voltage on the output capacitor by a certain amount, proportional to the drop across the converter's internal output impedance. If a high-speed comparator is used to detect when the output falls below a certain level, a hysteretic-type controller can be developed. With this simple control scheme, shown in figure 5.5, the output voltage can be held to a certain level while keeping ripple at a minimum.

The lower-bound feedback method does have several downsides that would have to be considered in any implementation. First, the comparator must be very fast to prevent the output from falling significantly below the reference. Second, if the output voltage remains below the reference after a switching event, or starts up below the reference, the comparator will be stuck on, preventing any switching action. Additional logic must detect this condition and inject a sufficiently-fast clock to boost the output voltage above the reference. The switching frequency using this lower-bound control method is bounded only by comparator speed, and is highly sensitive to noise. Noise also causes an increase in the magnitude of the voltage ripple, however the output maintains regulation regardless of noise.

The lower-bound hysteretic feedback method is used in the multi-ratio converter pre-

¹If a topology is chosen that transfers charge to the output during only one phase, a symmetrical topology can be created as in section 4.3.1 which transfers charge to the output on both phases.

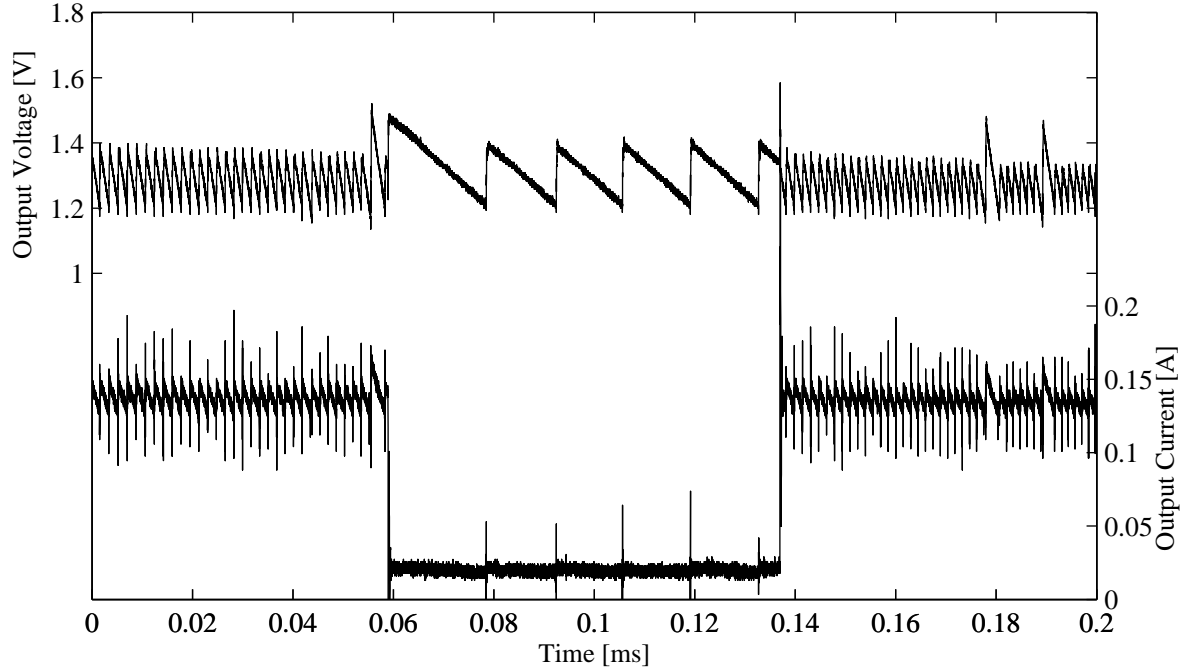


Figure 5.6. Waveform from lower-bound feedback-based converter

sented in section 5.4. A discrete-component prototype was developed with an integrated SC converter designed for handheld applications. Figure 5.6 shows the output voltage ripple (with a small output capacitor) as load current varies between full load and 10% load. At lower load currents, the ripple frequency falls proportional to the load, and the ripple amplitude gets slightly larger, as discussed in section 5.1. For this converter to be practical for many applications, the ripple amplitude would have to be reduced significantly via a larger output capacitor or multiple interleaved phases.

5.3 System Modeling

SC converters are typically regulated by varying switching frequency. This method of regulation yields inherently nonlinear dynamics which can be difficult to model. This section will develop a simplified model of an SC converter, enabling the design and simulation of control methods involving frequency modulation, pulse-width modulation and switch resistance modulation [18].

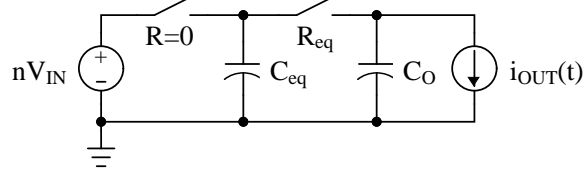


Figure 5.7. Idealized dynamics model for system modeling

The simplified circuit model for an SC converter used in this section is shown in figure 5.7. This model is the simplest model including the effects of both the SSL and FSL output impedance. The model uses a single capacitor of value C_{eq} to shuttle charge between the input and output ports with a series resistance R_{eq} . The output is modeled as a current source with bypass capacitance C_O . These equivalent component values can be found in terms of the SSL and FSL output impedances:

$$C_{eq} = \frac{1}{f_{sw} R_{SSL}}, \quad R_{eq} = R_{FSL}. \quad (5.3)$$

While this model is sufficient for modeling the control of many converters, an exact dynamic model is derived in appendix A.4. Each switching period will be modeled as a single sample in a discrete-time system. In each sample period, the output capacitor is linearly discharged by the output current source and charged through the RC network made with the flying capacitance and series resistance. A discrete-time system model can be made from this qualitative description as follows:

$$V_{OUT}[k+1] = V_{OUT}[k] + \frac{1}{C_O} \left(-i_{OUT}[k]T[k] + (nV_{IN} - V_{OUT}[k]) C_{eq} \left(1 - e^{-T/2R_{eq}C_{eq}} \right) \right) \quad (5.4)$$

where T is the duration of the switching period.

Since the primary method of regulation for SC converters is frequency modulation, the switching period T will be the primary control handle. In this section, the switch resistance R_{eq} will be held constant, although it can be varied linearly [18]. In addition, operation in the SSL will be assumed such that the exponential factor $1 - \exp(-T/2R_{eq}C_{eq})$ is equal to one.

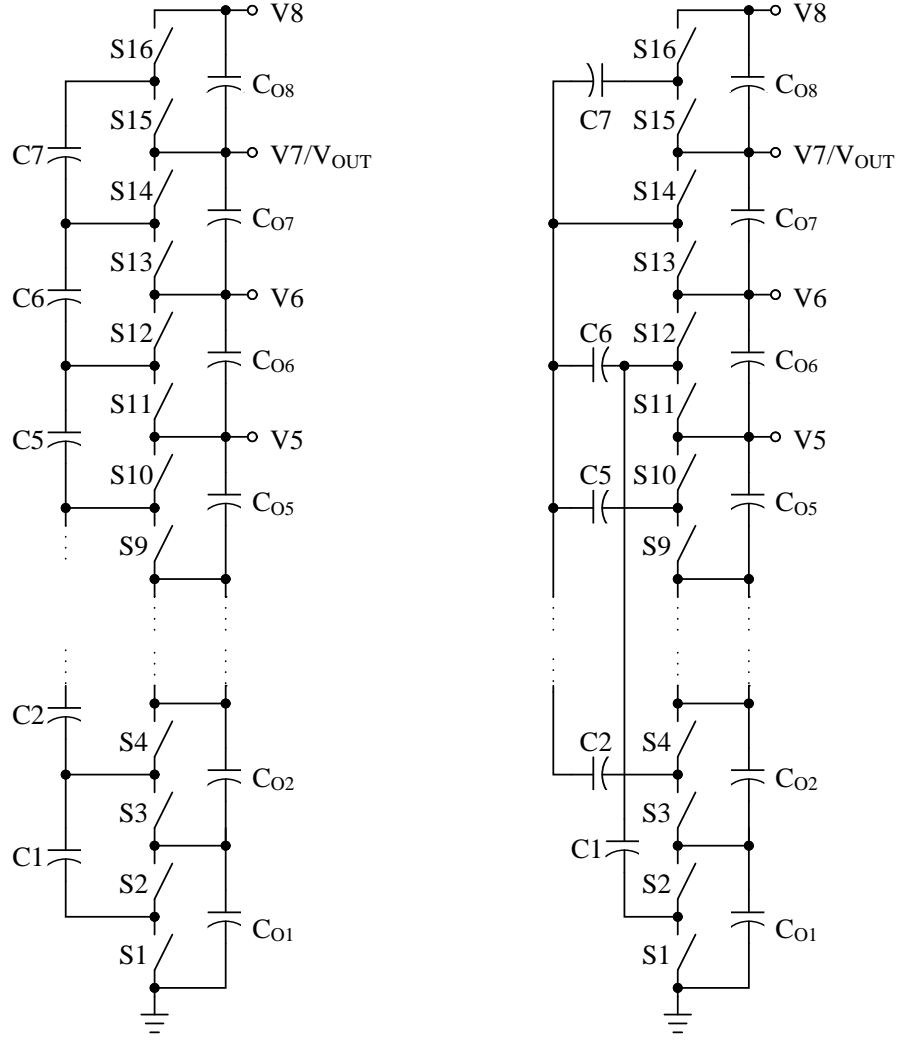
A compensator function $T = f(V_{OUT} - V_{REF}) = f(\epsilon)$ must be constructed to implement

the desired control law. Since the load current can vary over many orders of magnitude, and the relation between output voltage and period in (5.4) is nonlinear, a linear compensator function cannot guarantee stability and acceptable performance at all load levels. By inspecting (5.4), if the compensator function included the output current, the system can be made linear via feedback linearization. The use of a dynamic control method to regulate the output voltage requires the measurement or estimation of the output current to ensure stability and adequate performance.

If the compensator $f(\epsilon)$ is in the form $f(\epsilon) = f_2(\epsilon)/I_{OUT}$, the system becomes linear in terms of the new input $f_2(\epsilon)$. While $f_2(\epsilon)$ can be chosen to yield good dynamics, additional considerations will have to be made for a real system. For example, bounds on the switching frequency must be used and the dynamics of a VCO must also be considered. Finally, for correct operation, a limit to the slew rate of the output current must be made to ensure stability of the control system.

5.4 A Multi-Ratio Converter for Portable Electronics

The regulation methods for SC converters discussed so far have entailed modulating the output impedance to regulate the output voltage. These methods are inherently lossy and are only efficient near the optimal operating point of the converter. For a wide regulation range, a different method must be used. This section describes an SC converter designed for a portable electronics application where the input can vary between 2.1 and 4.8 V, an extended lithium-ion battery voltage range. The output of the converter is a constant 1.2 V to supply ICs fabricated in a deep sub-micron process. To ensure high (greater than 75%) efficiency over this range, numerous conversion ratios, in addition to the other regulation methods mentioned in this chapter, must be used. Multi-ratio regulated SC converters exist in commercial parts [43, 32], but are designed for neither ultra-high efficiency nor the use of integrated capacitors.



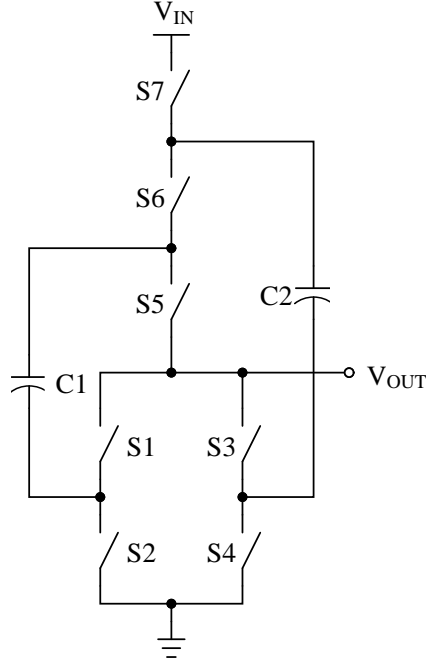
(a) nominal topology

(b) with transformed capacitors

Figure 5.8. $\{5, 6, 7, 8\}$: 7 ladder topology stage

5.4.1 Topology Description

To perform the conversion, a two-stage converter is used. The first stage, in figure 5.8, is an eight-rung ladder topology with an input multiplexer applying the input to one of four taps (denoted V5 through V8). The output is taken from V7 such that the ladder converter provides the conversion ratios 5:7, 6:7, 1:1 and 8:7. This intermediate rail is fed into the 3:1 Dickson converter, shown in figure 5.9a. By changing the way the switches are clocked, the Dickson stage can also perform a 2:1 conversion ratio. Thus, the two stages combined



Switch	3:1	2:1
S1	$\phi 1$	$\phi 1$
S2	$\phi 2$	$\phi 2$
S3	$\phi 2$	$\phi 1$
S4	$\phi 1$	$\phi 2$
S5	$\phi 2$	$\phi 2$
S6	$\phi 1$	ON
S7	$\phi 2$	$\phi 1$

(a) Dickson topology

(b) Switch phases vs. conversion ratio

Figure 5.9. 3:1, 2:1 Dickson topology stage

can provide the conversion ratios 10:7, 12:7, 2:1, 15:7, 16:7, 18:7, 3:1 and 24:7. These eight conversion ratios span the necessary input range nicely.

By using the two-stage design, many conversion ratios can be obtained at high efficiency. The first stage, while providing fine regulation, remains efficient since its conversion ratios remain close to 1:1. The ladder provides high efficiency at conversion ratios near 1:1, despite its drop in efficiency at higher ratios, as shown in section 4.2.1. The second stage provides the majority of the voltage conversion at relatively coarse 3:1 and 2:1 conversion ratios. However, the efficiency of the Dickson converter at these conversion ratios is high.

The capacitors in the ladder converter (in figure 5.8a) only support a fraction of a volt as shown. To achieve a better capacitor utilization, the capacitors are transformed to span the maximum number of rungs supported by the device's blocking voltage. The capacitor arrangement is optimized via computer iteration to determine the configuration with the lowest average sum of the capacitor charge multipliers. In this arrangement, each switching node remains connected to a capacitor, and each capacitor has one terminal at the node

shared by S13 and S14, when supported by the capacitor's blocking voltage. The result of this optimization is shown in figure 5.8b, and reduces the average sum of the capacitor charge multipliers by approximately 75%. The DC capacitors can also be reconfigured for optimal performance, but for this application, several of these topologies will be placed in parallel as interleaved phases, allowing the size of the DC capacitors to be significantly reduced. In this manner, the ladder stage has the minimal SSL impedance for a given capacitor die area.

The target process for this converter is a 65 nm CMOS process with the ability to accept a 5V I/O rail. In this design, metal-insulator-metal (MIM) capacitors are considered, as they are built in upper metal layers, and thus have low bottom-plate parasitic capacitances (approximately 0.3% to 1% of the main capacitance). Native NMOS transistors are used for both topologies, and are cascoded to block the necessary voltage to implement switch S6 in the Dickson stage. The gate of the cascode transistor of S6 can be biased via a doubled version of the output voltage (i.e. a constant 2.4 V). A die area of 3 mm² for both switches and capacitors is considered for a 100 mW application.

Figure 5.10 shows the calculated efficiency of this converter. The efficiencies of the optimal points for the eight configurations are shown as circles. By performing frequency modulation, regulation is possible over the entire range of input voltage. Since the optimal efficiency of the 15:7 configuration is below the regulation curve, it is globally inferior, and is thus never used.

5.4.2 Control Method

Performing output regulation with this converter is significantly more complicated than a single-ratio converter. An interior analog loop implements a lower-bound hysteretic control scheme to regulate the output voltage for a single configuration. A block diagram of the entire control scheme is shown in figure 5.11. The remainder of the controller is a finite state machine (FSM) to control the conversion ratio, implemented in the digital domain. Analog to digital converters (ADCs) convert the input voltage and output current to digital

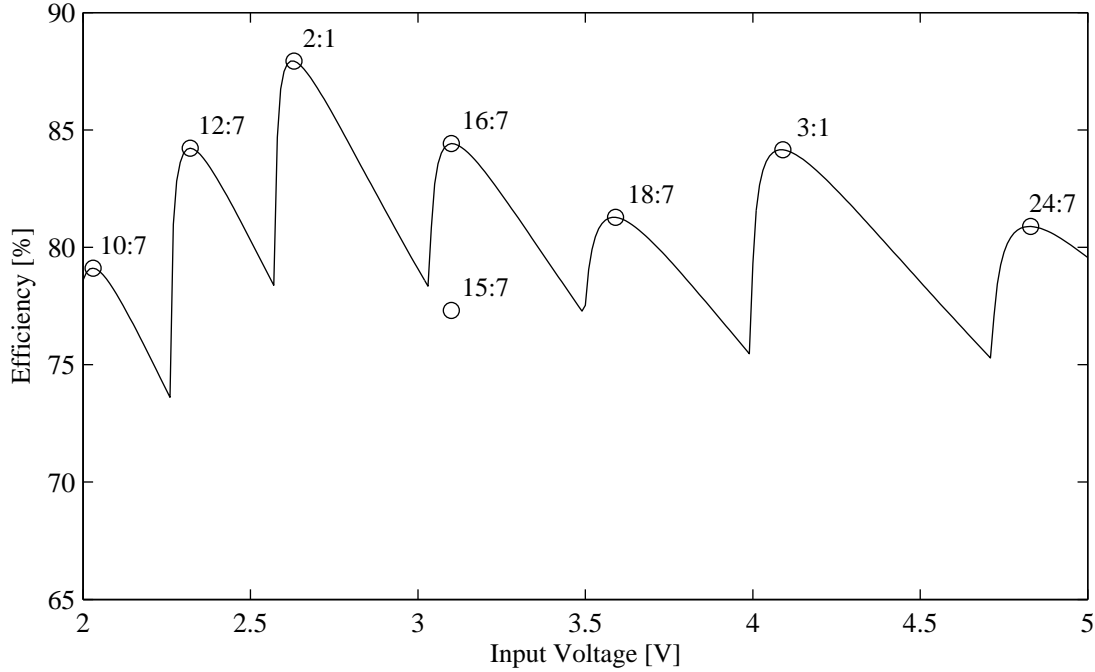


Figure 5.10. Predicted efficiency of multi-ratio converter

values. The output current then passes through a logarithmic filter, as only its approximate magnitude is important.

The first component of the digital control system is the frequency counter and comparator. The counter counts the number of phase transitions in a given period, set by a divided system clock. The maximum converter frequency is set by a constant maximum count. The maximum frequency comparator X6 indicates that the input voltage fell below the nominal range for the working configuration (or ratio), so the configuration must be changed to the next lowest conversion ratio. The comparator triggers the up/down counter to decrement the configuration by one step.

As the converter configuration is changed to a lower conversion ratio, the sampled input voltage is written in a look-up table (LUT) indexed to the previous configuration ratio and output current. The LUT stores the maximum input voltage to be used for the pre-transition configuration, based on the output current level. As the input voltage rises above this threshold for a given conversion ratio, the digital comparator X10 trips and triggers

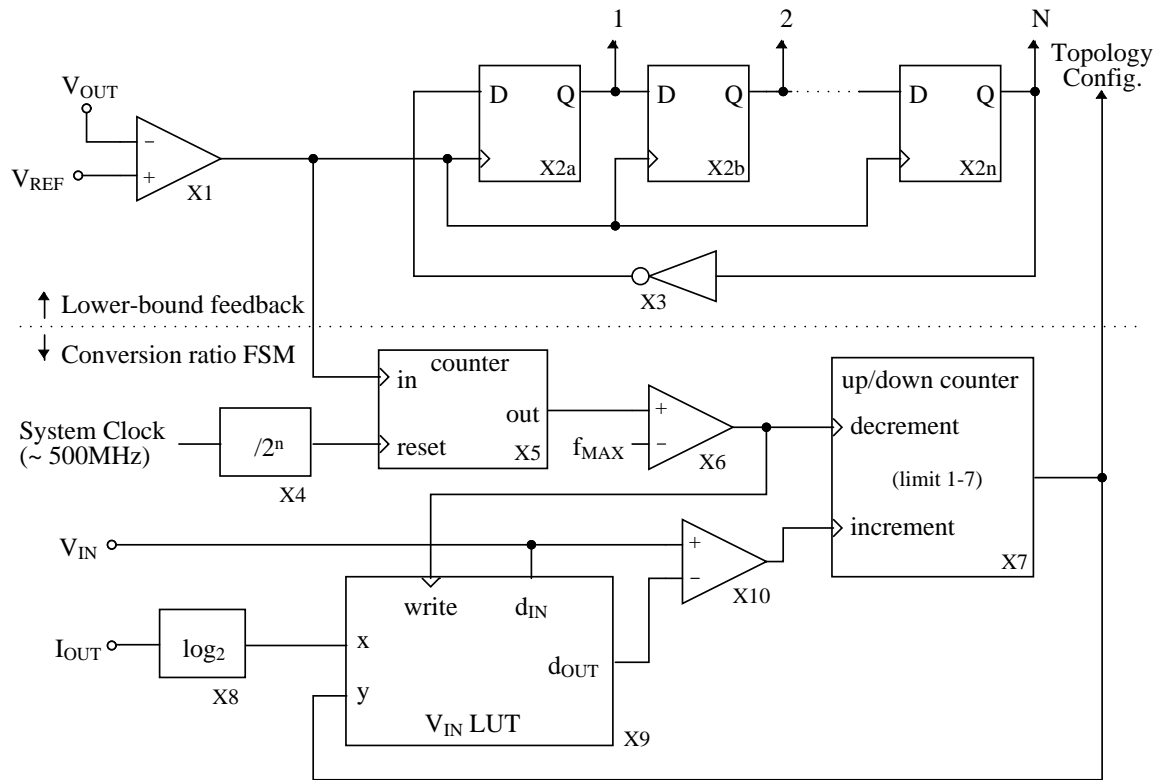


Figure 5.11. Controller for the multi-ratio converter

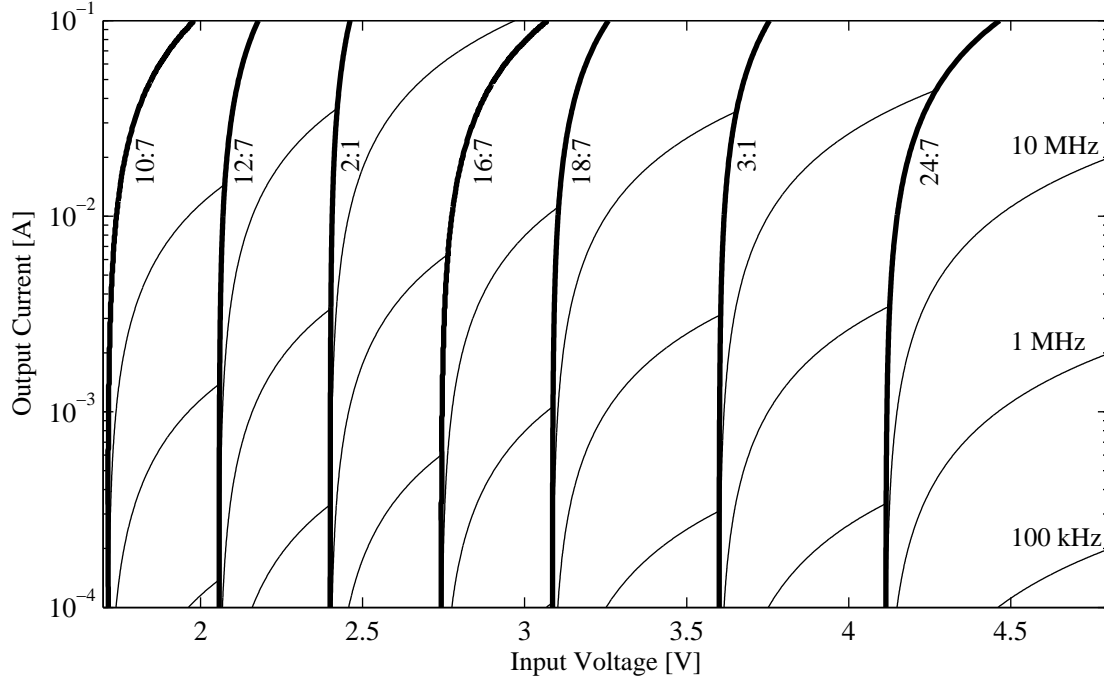


Figure 5.12. Operation regions for the multi-ratio converter

the up/down counter to switch to the next highest conversion ratio. Some hysteresis is incorporated into the system to avoid oscillation between conversion ratios. This system ensures the use of the proper conversion ratio across the input voltage range while using minimal digital resources. The control system could be improved by changing the maximum switching frequency based on output current to optimize the configuration transition points.

The operation of the converter, considering both switching frequency and conversion ratio, can be examined across the space of operation. Figure 5.12 shows this space with input voltage on one axis and output current on the other. The regions corresponding to each conversion ratio are shown separated by the dark lines. The conversion ratio transitions correspond to a maximum switching frequency threshold of 100 MHz. Three constant-frequency contours are also shown on this plot as narrow lines. This plot can be used to create a feed-forward control system by storing the correct conversion ratio or configuration in a fixed two-dimensional look-up table. The two-dimensional look-up table X9 stores this feed-forward data through on-line training.

5.4.3 Experimental Results

This design was not fabricated in the intended process, but a prototype was created using discrete components. The same voltage and power specifications were maintained, corresponding to similar switch conductance requirements. For ease of control, Maxim MAX4685 analog multiplexers were used for the power switches. The on-state resistance of each of these switches varies between $0.3 - 0.5$ ohms, suitable for this application. Two interleaved phases were used for the first stage, while four were used for the second stage to reduce output impedance and ripple magnitude. The capacitors were scaled up by a factor of approximately 500, from a few nanofarads to a few microfarads. Thus, the switching frequency is similarly reduced by a factor of 500 to a few hundred kilohertz.

The control was performed using a discrete op-amp, the National LMV7219, and an FPGA board based on a Xilinx Vertex 4 for the digital portion of the control. All the digital components of the control were implemented using Verilog. The test board also included a programmable input regulator and programmable load resistance for automated testing. The programmable source and load were also controlled by the same FPGA. The control logic occupied a very small fraction of the FPGA and could easily be synthesized and integrated onto the same IC as the power circuitry.

Figure 5.13 shows the efficiency and output voltage of running the converter at full load while varying the input voltage. While the mean output voltage varies due to varying ripple amplitude, the lower bound of the ripple is successfully regulated at 1.2 V. This is a consequence of the lower-bound feedback mechanism working as designed. The measured efficiency is between 45% and 80% for the majority of the input range. Since the gate drive power is included, the efficiency is lower than it would be for an integrated converter due to the use of the analog multiplexers as the power switches in the converter.

At low input voltages (less than 2.7 V), efficiency and output voltage drop significantly as the converter loses regulation. This phenomena can be explained due to the input being applied to the lower taps of the ladder converter at these lower input voltage levels. The

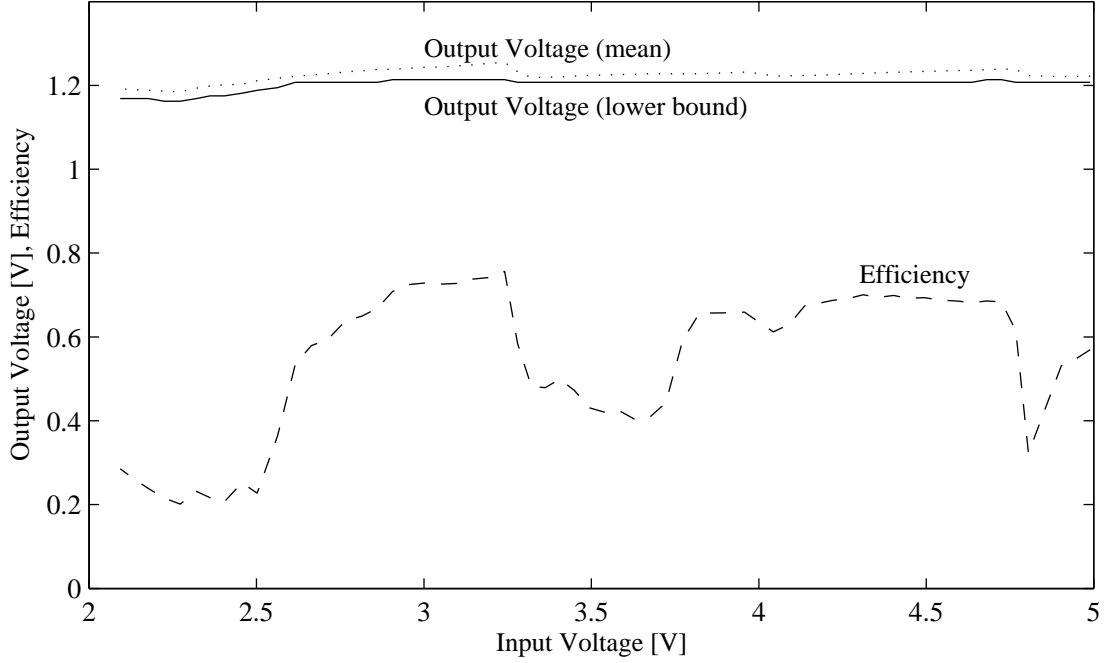


Figure 5.13. Output voltage and efficiency of the multi-ratio converter prototype

supply to the analog multiplexers is connected to the highest rail of the ladder converter. Since the resistance between the lowest rail (V5) and the highest rail (V8) is substantial, the converter is significantly loaded by the analog multiplexer supply. Thus, the intermediate voltage rail sags too much at low input voltage levels to maintain regulation.

The prototype results illustrates the functionality of the control scheme discussed in section 5.4.2. The output voltage ripple in this prototype was excessive due to few interleaved phases and minimal output capacitance. In an integrated converter, more interleaved phases would be used and if the loads are not on-chip, a small external bypass capacitor would be used to further control ripple. This topology is a promising development in on-chip voltage regulation for portable electronics.

Chapter 6

High-Voltage Converters for Airborne Robotics

Chapters 2 through 4 discuss the fundamentals of switched-capacitor converters, including a method of determining their output impedance and optimizing their performance. In addition, methods to regulate the output of SC converters was discussed in chapter 5. This complete design methodology can be applied to numerous examples. The first example, described in this chapter, uses a switched-capacitor converter to generate a high voltage supply for a piezoelectric-based airborne robot.

Micro air vehicles (MAVs) are small aircraft (typically less than 100 grams) which are often controlled autonomously [63]. These devices can be used for search-and-rescue, fire fighting, and numerous military applications. As these devices get smaller, cheaper and more maneuverable, their application space will increase dramatically. While current MAVs are typically fixed-wing aircraft or gliders, biologically-inspired designs have been more sparse. Insect-sized devices [62] require much higher power densities than previous MAV designs. Their implementation necessitates higher power density batteries and actuators and lightweight, high-efficiency power conversion. By making autonomous MAVs smaller

and cheaper, they can be used to distribute a dense wireless sensor network in hostile environments.

In [65], piezoelectric actuators were found to deliver the highest power density of any available actuator at the milligram-level. However, these actuators, typically made with lead zirconate titanate (PZT), require actuation voltages of 150–300V. Generating this voltage from a typical MAV power source, a lithium-ion battery at 3.7V, is a difficult problem. While the entire energy chain has been examined in [57], the power electronics design will be examined in detail in this chapter.

Topologies for generating a high voltage at a high conversion ratio will be investigated, using both magnetics-based and switched-capacitor-based solutions. By comparing various power-conversion topologies in terms of both efficiency and weight, an optimal design will be developed. Three power converters for this purpose are shown in figure 6.1. For each topology, specific discrete components are chosen to illustrate the weight, efficiency and feasibility of each design. The analysis method in chapter 2 is used in part to determine the performance of these converters.

After topologies for high-ratio conversion have been discussed, the MicroGlider project will be described, including the specifics on the converter used for this project. This MicroGlider has a mass of two grams with an on-board lithium-polymer battery, microcontroller, flight sensors, charge pumps, power amplifiers and actuators. In addition, a RFID payload was incorporated into the wing for remote tracking.

6.1 Comparison of Topologies for Lightweight High-Voltage DC-DC Converters

This section will analyze several high-voltage DC-DC converter topologies in terms of efficiency and component mass. For analysis purposes, the masses of common surface-mount type devices are shown in table 6.1. This mass does not include solder or the PCB area occupied. These two additions will increase the total weight of a properly designed

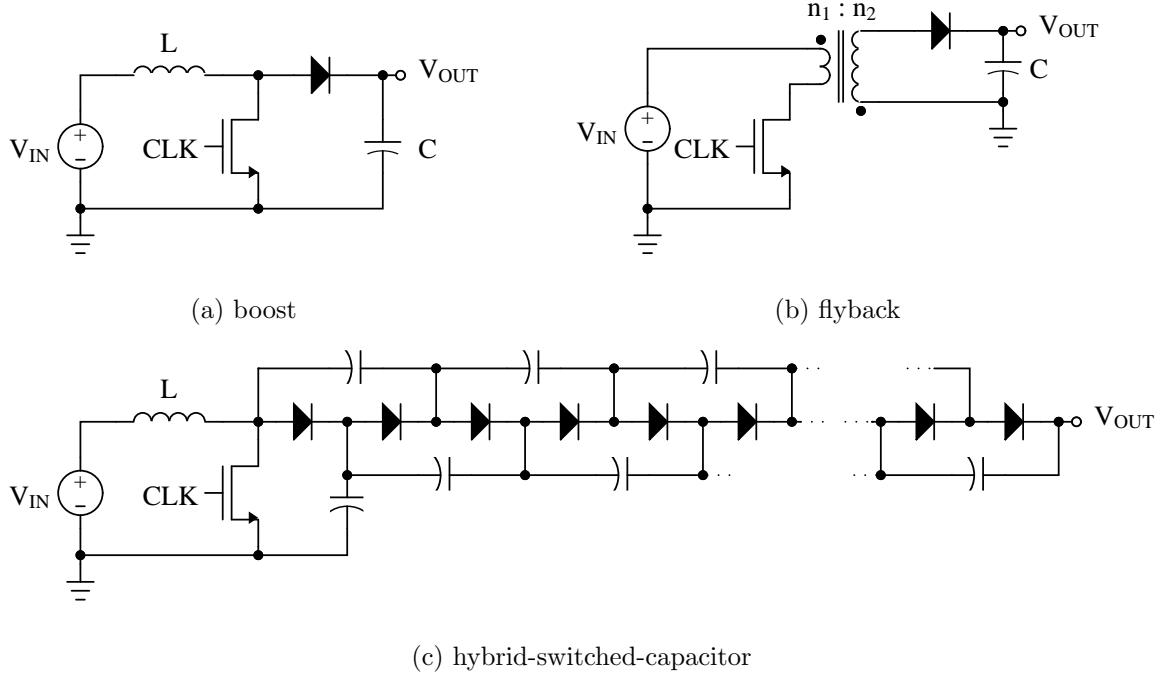


Figure 6.1. Three topologies for lightweight, high-voltage DC-DC conversion

and soldered circuit board by 50–100%. The power inductors weigh more than the other components as they contain a substantial amount of ferrite or other iron-based material. Next, it is important to know the available capacitance and inductance values for various package types and working voltages (for capacitors) or saturation current (for inductors). Graphs showing the capacitance and inductance density of several miniature surface-mount components are shown in figure 6.2. It is interesting to note that these components have approximately constant volumetric energy density across the range of blocking voltages or saturation currents.

The passive actuation for the MicroGlider in section 6.2 requires an output power level of 10 mW. However, if an insect-inspired actively flying robot is made, it would require an electrical power of 111 mW per gram robot mass to provide lift [57]. Designs will be compared for a 200V output at both 10 mW and 222 mW (for a two-gram aircraft).

Category	Package	Mass	Notes
Resistors	0402	0.6 mg	
	0603	2 mg	
	0805	5 mg	
Capacitors	0402	2 mg	
	0603	5–6 mg	Mass measured
	0805	15 mg	
Inductors (Coilcraft)	0603PS	27 mg	
	0805PS	60 mg	
Inductors (Taiyo-Yuden)	0603	11 mg	Mass estimated from
	0805	27 mg	mechanical diagram
Silicon components	SOT-23	8 mg	
	SOT-23-6	15 mg	Mass measured
	SOT-363	7 mg	

Table 6.1. Mass of common surface-mount components

Voltage Level	Device	$V_{DS,max}$	$R_{DS,on}$	C_D
High Voltage	Supertex TN2124	240 V	15 Ω	9 pF
	Supertex TN2425	250 V	3.5 Ω	25 pF
Medium Voltage	Fairchild 2N7002	60 V	5 Ω	11 pF
	Zetex ZXMN6A07F	60 V	0.35 Ω	19.5 pf

Table 6.2. N-channel MOSFETs in SOT-23 package

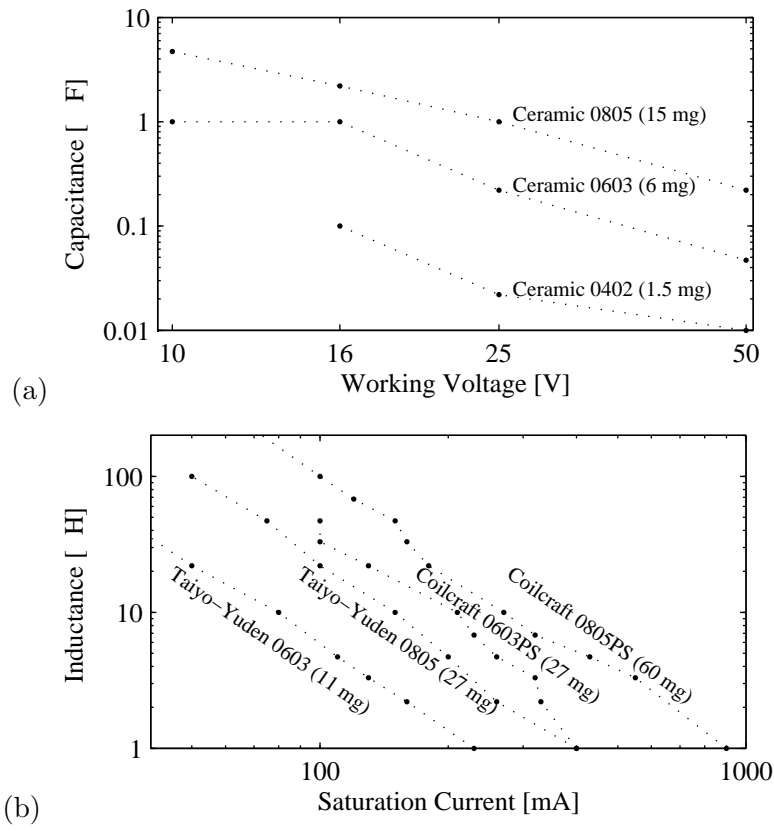


Figure 6.2. Available (a) capacitors by voltage and (b) inductors by current

6.1.1 Boost Converter

A boost converter, shown in figure 6.1a, is the simplest DC-DC converter which can be used to generate the 200V required to run the piezoelectric actuators. In this analysis, operation in discontinuous conduction mode (DCM) will be assumed. In each switching period, the transistor turns on for time t_{on} and magnetizes the inductor to a peak current, denoted I_{pk} . The switch then turns off and causes the inductor current to flow through the diode, charging the output capacitor, until the inductor current reaches zero. In the charge-up phase, the peak current can be found in terms of the inductance, battery voltage, and on-time:

$$I_{pk} = t_{on} \frac{V_{IN}}{L}. \quad (6.1)$$

The charge delivered to the output can be similarly found in terms of the peak current:

$$Q_{OUT} = \frac{1}{2} I_{pk} t_2 = \frac{1}{2} I_{pk} \left(\frac{I_{pk} L}{V_{OUT} - V_{IN}} \right) \quad (6.2)$$

where t_2 is the time that the inductor current ramps down to zero through the diode. Next, (6.2) will be multiplied by f_{sw} to obtain the output current in terms of system parameters and peak inductor current. Then the inductance will be found in terms of peak current and system parameters to find the application tradeoff between inductance and peak inductor current:

$$L = 2 \frac{(V_{OUT} - V_{IN}) i_{OUT}}{f_{sw} I_{pk}^2}. \quad (6.3)$$

Since the output voltage in this application is much larger than the input voltage, by approximating $V_{OUT} - V_{IN} \approx V_{OUT}$, (6.3) can be transformed into a relation between load power and peak inductor energy storage:

$$\frac{1}{2} L I_{pk}^2 \approx \frac{P_{OUT}}{f_{sw}}. \quad (6.4)$$

Thus, given an inductor peak energy and output power, the converter's switching frequency can be found. However, it may be more efficient to run the converter at a lower peak current. At a lower peak inductor current, while the switching frequency increases, the inductor core loss may decrease such that the overall efficiency is higher. To minimize inductor mass, it is likely that the inductor is operated near the saturation current.

To calculate efficiency, the converter losses must be analyzed. Three losses will be considered in this exploratory analysis. The on-state resistance loss and drain-source capacitance loss of the MOSFET depends on choice of MOSFET and the other design parameters. The inductor ESR loss of the inductor will also be considered. Since the inductor loss and on-state resistance loss are both resistive, they will be considered together as a lumped resistance R :

$$P_{RES} = \overline{i^2 R} = f_{sw} R \int_0^{t_{on}+t_2} I_L(t)^2 dt \quad (6.5)$$

where I_L is the inductor current. Since the inductor current ramps up linearly to I_{pk} over time t_{on} , (6.5) can be integrated:

$$P_{RES} = f_{sw} R \frac{t_{on} + t_2}{t_{on}} \int_0^{t_{on}} \left(\frac{t}{t_{on}} I_{pk} \right)^2 dt = \frac{1}{3} f_{sw} (t_{on} + t_2) R I_{pk}^2. \quad (6.6)$$

By realizing the input current i_{IN} is the time-averaged inductor current, the input current can be written as:

$$i_{IN} = \frac{1}{2} I_{pk} f_{sw} (t_{on} + t_2). \quad (6.7)$$

A final expression for the resistive power loss is then given by:

$$P_{RES} = \frac{2}{3} i_{IN} I_{pk} R. \quad (6.8)$$

Likewise, the drain-source capacitance loss of the MOSFET can be represented as:

$$P_{CAP} = f_{sw} C_D V_{OUT}^2 \quad (6.9)$$

since the MOSFET's blocking voltage is approximately equal to the output voltage.

The two primary losses stated here must be optimized by choosing the inductor, MOSFET and switching frequency. Table 6.2 shows a number of high- and medium-voltage MOSFETs for use in these converters. Since the boost converter places a large blocking voltage requirement on the power switch (200V), only the high-voltage switches can be used for this application.

By choosing the highest available inductance in a series, the peak current is kept minimal (presuming $I_{pk} > 2i_{IN}$ to maintain DCM operation). For each inductor type and load, the

Power Level	Taiyo-Yuden	Taiyo-Yuden	Coilcraft	Coilcraft
	0603	0805	0603PS	0805PS
	(11 mg)	(27 mg)	(27 mg)	(60 mg)
10 mW				
Switch Type	TN2124	TN2124	TN2124	TN2124
Inductance	10 μH	47 μH	47 μH	330 μH
Switching frequency	312 kHz	75.6 kHz	42 kHz	17 kHz
Peak Current	80 mA	75 mA	100 mA	60 mA
Power Loss	115 mW	30 mW	19.3 mw	10 mW
Efficiency	8.0 %	25.2%	34.2%	49.7%
220 mW				
Switch Type	N/A	N/A	TN2124	TN2124
Inductance	N/A	N/A	0.78 μH	3.9 μH
Switching frequency	N/A	N/A	763 kHz	456 kHz
Peak Current	N/A	N/A	860 mA	529 mA
Power Loss	N/A	N/A	824 mW	492 mW
Efficiency	N/A	N/A	21.1 %	30.9%

Table 6.3. Efficiency of single-stage boost converter

optimal switch type is chosen and peak current optimized to yield the optimal design. At this optimal design point, the power loss and efficiency are evaluated. Table 6.3 shows the efficiency of these designs. By choosing the most-efficient design with a suitable component weight (including control components), the optimal design can be obtained.

However, after inspecting the designs, none of the potential designs result in an acceptable efficiency at an acceptable mass. Since the power switch must conduct the input current but block the output voltage, it has a very large V-A product, which results in large switch dissipation. To improve the efficiency, converters that stress the power switches less will be utilized. Two boost converter stages could be cascaded, such that the conversion

ratio of each converter is modest. While this method may yield increased efficiency, the mass of the additional inductor and control circuitry would make the converter prohibitively heavy. A flyback converter and a hybrid switched-capacitor converter will be used to lower the switch stresses while using only a single magnetic element.

6.1.2 Flyback Converter

A flyback converter, as shown in figure 6.1b, is a transformer-based indirect converter. The transformation ratio n_2/n_1 greatly lessens the switch stresses on the primary-side switches, allowing a greater efficiency. When the power switch is on, the current in the magnetizing inductance of the transformer ramps up linearly at a rate proportional to the input voltage. When the switch turns off, the magnetizing inductance current ramps down through the transformer to the output. In this configuration, the power switch nominally blocks a voltage equal to $V_{IN} + (n_1/n_2) V_{OUT}$. An additional margin must be included in the switch voltage rating due to effects of the transformer's leakage inductance. With a turns ratio of 1:50, and an output voltage of 200V, the reset voltage of the transformer equals 4 V. When the reset voltage is added to the battery voltage, the power switch blocking voltage is approximately 8 V (discounting the effect of the leakage inductance), allowing the use of a 20 V switch.

While the switch stresses are greatly reduced in a flyback converter, the design of the transformer becomes the largest issue in implementation. Power inductors are typically custom-wound for a particular application from commercially-available magnetic cores. In this application, the smallest available cores must be used. For this explorative calculation, the MicroMetals T14-26A toroidal core will be used, with a mass of 77mg. Smaller cores are available for RF and EMI applications, but their suitability for power applications is unknown. The ungapped core exhibits a single-turn inductance of 12.5 nH and outer and inner diameters of 3.43 and 1.70 mm, respectively.

Winding the transformer also presents great difficulty as the inner aperture is very small and the turns ratio is very large. The number of turns on the primary is computed

	10 mW	220 mW
Switch Type	ZXMN6A07F	ZXMN6A07F
Switching frequency	13 kHz	289 kHz
Peak current	550 mA	550 mA
Power loss	0.79 mW	17.3 mW
Efficiency	92.7 %	92.7 %

Table 6.4. Efficiency of flyback converter using custom transformer

by optimizing power loss using a reasonable switching frequency. For a modest 20 primary turns, 1000 secondary turns are necessary, requiring very fine-gauge wire. The feasibility of winding such a transformer will be neglected, although it would be a non-trivial aspect of any implementation. If 75% of the aperture is used for the secondary, at a 50% packing factor, the secondary wire must have a diameter less than 0.033 mm. AWG 48 wire needs to be used for the secondary, with a resistance of $21.8 \Omega/m$. The resistance of the secondary would equal 240Ω . Reflecting this impedance to the primary yields $96 m\Omega$. Similarly, the primary winding is specified with AWG 36 wire, with a total resistance of $290 m\Omega$. The total mass of these two windings equals 108 mg, dominating the mass of the converter.

The maximum magnetic field for the toroid material is 0.6 tesla before significant saturation occurs. However, for efficiency, the field will be restricted to 0.2 T. This flux limit corresponds to a primary current limit of 0.96 A. However, the optimal peak current will likely be less than this limit, as was the case for the boost converter. To find the optimal operating conditions for the converter, the same method as the boost converter will be used. However, as the magnetic component is now fixed, only the switches in table 6.2 can be adjusted, along with the peak current. The efficiency of the flyback converter, using this transformer, is shown in table 6.4. Switch resistive and capacitive losses are considered, as well as transformer core and copper losses.

The flyback converter achieves a very high efficiency when compared with the boost converter. However, the manufacturing of this transformer would be extremely difficult,

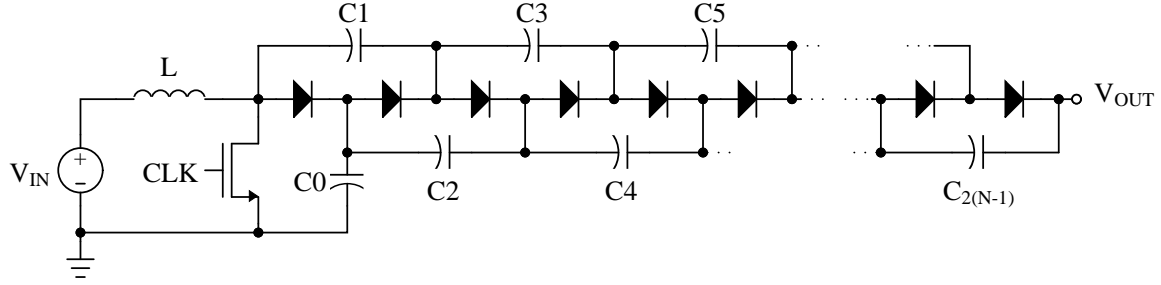


Figure 6.3. Hybrid switched-capacitor boost converter

and its mass should be reduced further for practicality. Additionally, the mass and power consumption of the necessary control circuitry have not been considered. Since this converter is impractical for prototyping (and likely manufacture), an alternative is considered in section 6.1.3. The hybrid switched-capacitor converter combines the low switch stress of the flyback with use of only off-the-shelf components.

6.1.3 Hybrid Switched-Capacitor Boost Converter

The hybrid switched-capacitor converter was developed to reduce the switch stresses of the boost converter's MOSFET while maintaining use of off-the-shelf components in a single converter. A pure switched-capacitor circuit could be designed to do the conversion, but as the conversion ratio is large, a prohibitively large number of components would be needed. The hybrid SC-boost converter, shown in figure 6.3, uses a boost converter to generate an intermediate voltage (about 30 V) and to drive a passive, diode-based charge pump to generate the desired 200 V output.

For simplicity, the efficiency of the boost converter and SC converter will be analyzed independently. First, the boost converter will be examined with a standard resistive load. The method presented in section 6.1.1 will be used here when considering the devices in table 6.2 and figure 6.2. For the low-power converter, the Coilcraft 0603PS inductor series will be used. Similarly, the 0805PS series will be used for the high-power case. After optimizing the boost converter at the two power levels, the design parameters and results are shown in the top half of table 6.5.

The low-ratio boost converter stage is significantly more efficient than the high-ratio boost converter in section 6.1.1. Due to the lower switch stresses of this design, the boost converter exhibits high efficiency with modest part mass. Next, the efficiency SC converter stage will be considered.

The SC converter component of this hybrid converter is a ladder converter attached to the boost converter across the rectifying diode. The rectangular waveform across this diode allows the charge pump to operate without any active or controlled components. Three losses will be considered: the SSL output impedance loss, the cascaded diode voltage drop and the diode junction capacitance loss.

The structure of the ladder topology allows each capacitor to only support the input voltage, in this case 30V. Thus, instances of the same part can be used for all capacitors, although for increased power capability, the capacitors near the input can be doubled up in parallel to approximate the optimal capacitor sizings from section 3.2.1. However, we will consider all capacitors to be identical, as that assumption yields the least mass. The SSL impedance of the ladder converter is proportional to the sum of the squares of the capacitor charge multipliers, as found in section 2.1:

$$R_{SSL} = \sum_{i \in caps} \frac{(a_{c,i})^2}{C f_{sw}} \quad (6.10)$$

where N is the number of stages, C is the value of each capacitor, and f_{sw} is the switching frequency of the boost converter since the charge pump operates at the same frequency as the boost converter. For an N -stage ladder converter, there are two chains of $N - 1$ capacitors, each with charge multipliers increasing by integers from 1 to $N - 1$. By adding the squares of these components, the SSL output impedance can be found:

$$R_{SSL} = \frac{1}{C f_{sw}} \frac{2N^2 - 3N^2 + N}{3} \quad (6.11)$$

where N is the number of stages and C is the value of each of the capacitors in the converter.

Next, diode loss will be considered. As diodes are modeled as voltage drops, not resistive drops, the FSL impedance model cannot be used. For this converter, the BAS40DW-04 diode from Diodes, inc. is used as it supplies four series-connected diodes in a 6-pin 7 mg

		10 mW	220 mW
Boost	Switch Type	ZXMN6A07F	ZXMN6A07F
	Inductance	10 μH	3.3 μH
	Switching frequency	45 kHz	485 kHz
	Peak current	210 mA	580 mA
	Power loss	1.6 mW	25.5 mW
	Efficiency	86.4%	89.6%
Switched-capacitor	Capacitor Type	10nF 0402	47nF 0603
	Diode type	BAS40DW-04	BAS40DW-04
	Number of stages	8	7
	Output Voltage	207 V	199 V
	Efficiency	79.2%	90.1%
Total	Efficiency	67.9%	80.7%
	Component mass	85 mg	176 mg

Table 6.5. Efficiency of hybrid boost converter

SOT-363 package. These Schottky diodes exhibit a breakdown voltage of 40 V and forward voltage of 0.35 V at 1.0 mA. Capacitor C1 in figure 6.3 is charged from capacitor C0 with a single diode drop. In each phase, the two chains of capacitors equalize through the diodes. Since in each phase, the on-state diodes conduct the same current in the same direction, the diode forward drop does not yield a decreasing set of capacitor voltages. Instead, each capacitor in the open-circuit case nominally equilibrates to the output of the boost converter minus a single diode drop.

Finally, the diode junction capacitance loss originates from each diode turning on and off each period, charging and discharging the parasitic junction capacitance. For the BAS40DW-04 diode, it has a cumulative junction charge of 52 pC at 30 V. Thus, for each switching period, 1.56 nJ of energy is lost per diode. This loss is incorporated into the numbers in table 6.6. The loading of the diode junction capacitances is incorporated into the model as an additional output current with similar power consumption. This approximation overestimates the loading due to the diode capacitances, and is thus a worst-case bound.

Table 6.6 shows the output voltage and efficiency of the ladder converter for a range of stages. In these calculations, the 10 mW converter design is considered using 10 nF 0402 capacitors and a 30 V boost converter output. The output resistance is adjusted to yield 10 mW output power at each number of stages. As the number of stages increases, the incremental voltage gain decreases and the efficiency drops. For this application, eight stages will be used, as it provides an output closest to 200 V.

The total converter efficiency is shown in table 6.5. The mass of the switched-capacitor converter adds only 50 mg to the mass of the 35 mg, 10 mW boost converter and 108 mg to the 68 mg, 220 mW boost converter. The efficiency of the converter can be increased by increasing the switching frequency (by decreasing the inductance value of the boost converter). The hybrid SC-boost converter provides a relatively light and efficient converter for aerial robotics without the need for a heavy custom-wound transformer. The implemen-

Stages	Output impedance	Load resistance	Output voltage	Efficiency
4	62.2 k Ω	1.3 M Ω	113.4	90.3%
5	133 k Ω	1.9 M Ω	139.0	87.5%
6	244 k Ω	2.7 M Ω	163.3	84.8%
7	404 k Ω	3.5 M Ω	186.2	82.0%
8	622 k Ω	4.3 M Ω	207.5	79.3%
9	907 k Ω	5.2 M Ω	227.5	76.5%
10	1.27 M Ω	6.0 M Ω	245.1	73.7%

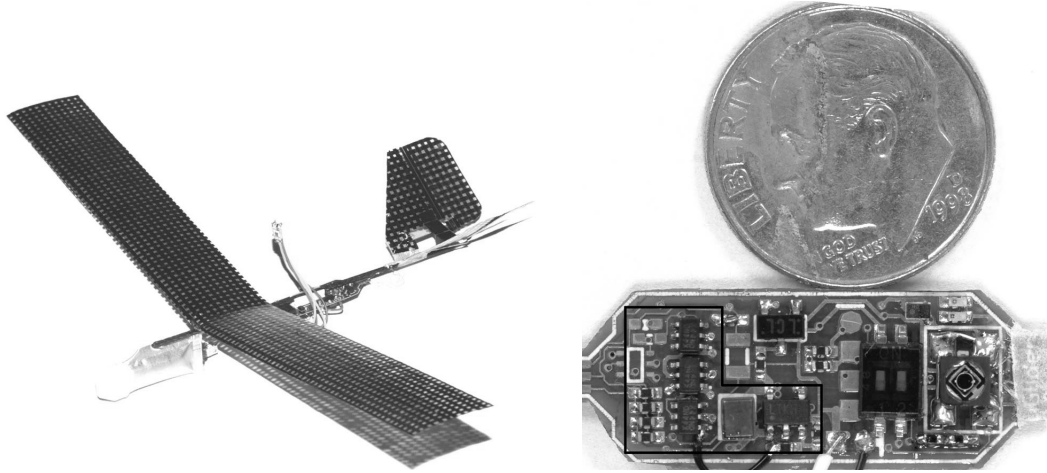
Table 6.6. Efficiency of ladder converter with 4–10 stages at 10 mW load

tation of this hybrid SC-boost converter topology will now be examined as it is used in the MicroGlider project.

6.2 MicroGlider Power Converter

The MicroGlider is a two-gram passive aircraft used for remote sensing purposes [64, 63]. A box of these gliders can be released from a piloted aircraft above territory where access is impossible or impractical. The gliders slowly spiral down until a target or destination is located. Then the glider steers itself to that point to position a wireless sensor node (in the experimental prototype, an RFID tag) on the target. The glider is made with carbon fiber wings and control surfaces with a carbon-fiber tube fuselage. A 20 mAh lithium-polymer battery is used as the power source, and is located at the front of the plane (with an attached wire bumper) for balance. The control PCB contains all the control and power electronics and is centrally located on the fuselage. The glider and the control PCB are shown in figure 6.4.

The MicroGlider uses a hybrid SC-boost power converter to generate the 200V bias rail for the power amplifiers to drive the piezoelectric actuators. The converter used is shown in figure 6.5. A Linear Technology LT1615-1 boost converter controller chip was



(a) Carbon fiber MicroGlider[64]

(b) Control PCB; power converter outlined

Figure 6.4. Photos of the MicroGlider and control PCB

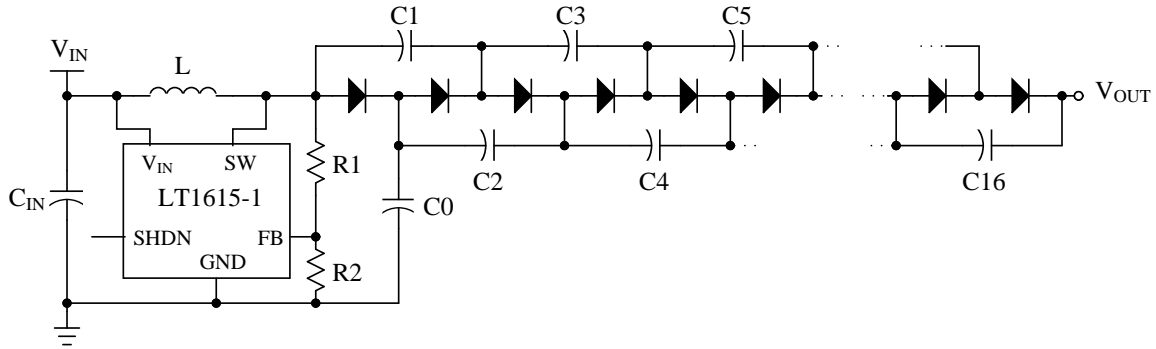


Figure 6.5. Hybrid SC boost converter as appearing on the MicroGlider

used to generate the intermediate 30V rail and to drive the nine-stage ladder topology. An intermediate output tap was provided at seven stages in case a lower voltage, higher-efficiency supply was desired.

The LT1615-1 part automatically controls the boost controller with feedback supplied by the resistor divider made with R1 and R2. A Coilcraft 10 μH 0603PS shielded ferrite inductor was used for the boost converter component. When the output voltage falls below the threshold, the inductor is magnetized through the internal switch to a trip point of 100 mA, then turned off (with a 400 ns delay). The SC ladder topology is identical to the one discussed in section 6.1.3 using BAS40DW-04 diodes and 10 nF 0402 capacitors. The

Load	7 stages		9 stages	
	10 M Ω	3.3 M Ω	10 M Ω	3.3 M Ω
Output Voltage	162.3 V	160.7 V	203 V	200 V
Output Power	2.63 mW	7.83 mW	4.12 mW	12.1 mW
Efficiency	51.5%	61.3%	47.5%	51.8%
Output impedance	49.2 k Ω		49 k Ω	

Table 6.7. Experimental results of the MicroGlider converter

converter IC runs from an input as low as 1.0 V, suitable for a lithium-ion battery, and can output up to 35 V. With a quiescent current of 19 μ A, the control circuitry does not significantly affect efficiency. For a 20 V, 10 mW output, the measured efficiency of the stand-alone boost converter is 73% [26]. The feedback network (R1 and R2) were tuned to deliver an intermediate voltage of 31 V.

When cascading a seven-stage ladder converter with this boost converter, an overall efficiency of 59.9% at an output voltage of 186 V is expected. With nine stages, the calculated efficiency and output voltage are 55.8% and 227 V, respectively. The converter was fabricated using a 3-mil-thick flexible PCB and occupies 0.8 cm² of board area on the control PCB. It was tested using a 3.5V voltage source and a resistive load.

The output voltage and efficiency of the fabricated converter are shown in table 6.7. The efficiency and output voltage numbers are quite close to the predicted values, with the output voltage sagging some due to the un-modeled loading from the diode junction capacitance. The incremental output impedance numbers do not match those given in table 6.6 as the boost controller automatically increases switching frequency as load current increases. In conclusion, the hybrid boost converter is an efficient method to generate high voltages in a mass-constrained application using off-the-shelf components.

Chapter 7

Switched-Capacitor Converters for Wireless Sensor Nodes

Switched-capacitor converters exhibit many advantages over traditional inductor-based converters for ultra-low-power applications. This chapter examines the power processing circuitry designed for a miniature energy-harvested wireless sensor node (WSN). Switched-capacitor converters are ideal for WSNs as they can easily be integrated and have high efficiency over a wide range of power levels.

Wireless Sensor Nodes (WSNs) are using less power and are becoming smaller as this technology matures. Scavenged-power sensor nodes are now a reality with modern processor, sensor and radio technology [38, 45]. While energy harvesters and their power conversion circuits have recently been integrated on the same die [29], the power harvested is not yet sufficient to power a 1-10 μW sensor node. By using MEMS energy harvesters [44] and inkjet printed super-capacitors and batteries [55, 56], a highly-capable sensor node can be made in the size of a sugar cube (1 cm^3) [39].

The efficiency of the scavenger-battery-load power interface path, especially at low power, is critical to the performance of such a sensor node. This chapter discusses the

design of a custom IC to perform scavenger-to-battery and battery-to-load power conversion, while meeting power and size constraints of the system.

7.1 Application and IC Overview

This chapter describes a power interface integrated circuit [52, 49] for a wireless tire pressure sensor (TPS), running from energy scavenged from a magnetic shaker [38, 11]. Photos of the node and scavenger are shown in fig. 7.1, with dimensions indicated. The sensor node is a modular stack of 1 cm^2 printed circuit boards connected by elastomer connectors. Each board contains a single functional block of the system. The energy consumers, or loads, include a TI MSP430 microcontroller, an Infineon pressure and acceleration sensor, and a custom PicoRadio radio transmitter [12]. The microcontroller and sensor run at a minimum 2.1 V supply and the radio requires a precise 0.65 V supply. A small NiMH coin cell with a nominal capacity of 18 mAh is used as an energy buffer, although the use of a supercapacitor is also feasible. The electromagnetic shaker utilizes the rotation of the tire to generate energy to power the sensor.

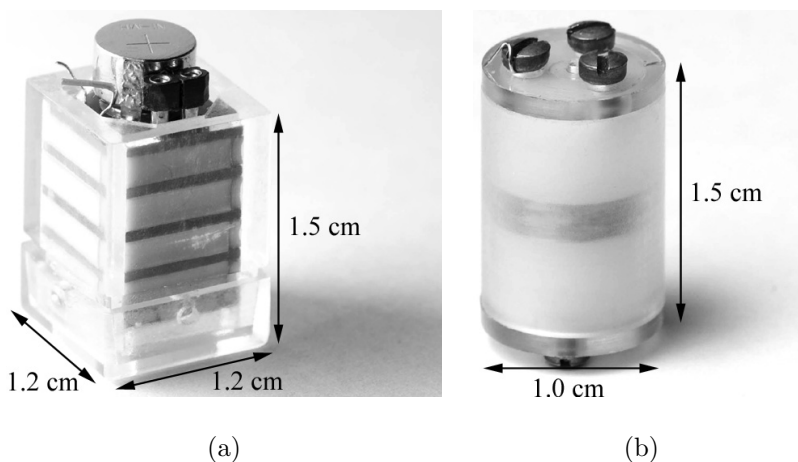


Figure 7.1. Photos and dimensions of the a) PicoCube and the b) electromechanical shaker

WSNs often run at very low duty cycles to minimize power consumption. In the TPS application, tire pressure is measured once every six seconds. Power consumption for a

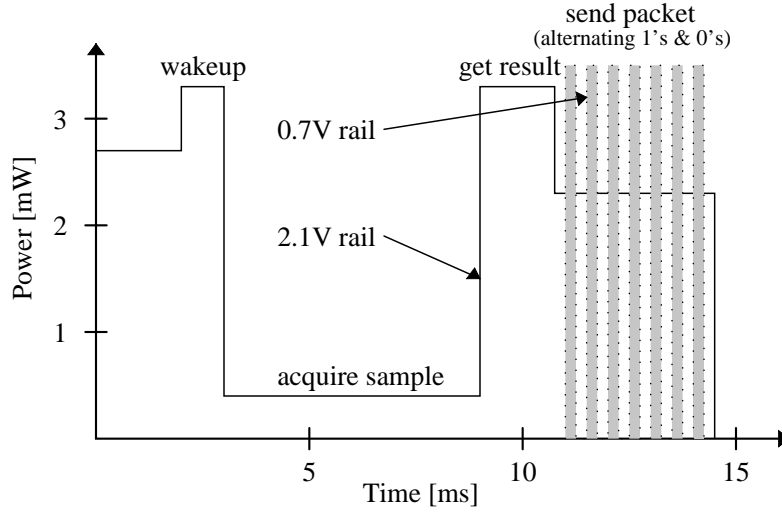


Figure 7.2. Measurement and transmission power

single 14ms measurement/transmission period is shown in figure 7.2. Each 14ms measurement/transmission cycle uses approximately $29 \mu\text{J}$, yielding peak powers of several mW. Node standby power is less than $1 \mu\text{W}$ resulting in a time-averaged power consumption of approximately $6 \mu\text{W}$.

The performance of a self-powered WSN is often defined by the sample rate or the number of samples per second the node can acquire and transmit. For a given fixed energy per packet, and a fixed average power supply (defined by the capabilities of the battery or energy scavenger), the sample rate is highly dependent on the efficiency of the power interface circuits. Since WSNs spend the vast majority of time in standby mode, power efficiency at microwatt levels is critical but lacking in current solutions. This power interface IC aims to improve this efficiency.

The architecture of the power interface IC is given in figure 7.3. The synchronous rectifier interfaces the electromagnetic shaker (harvester), which puts out a pulsed waveform, to the battery. Details about its use and implementation are in section 7.4. Two switched-capacitor power converters convert the battery voltage, nominally 1.2 V, to 2.1 V for the microcontroller and sensors and to 0.7 V to power the radio. The design of the power

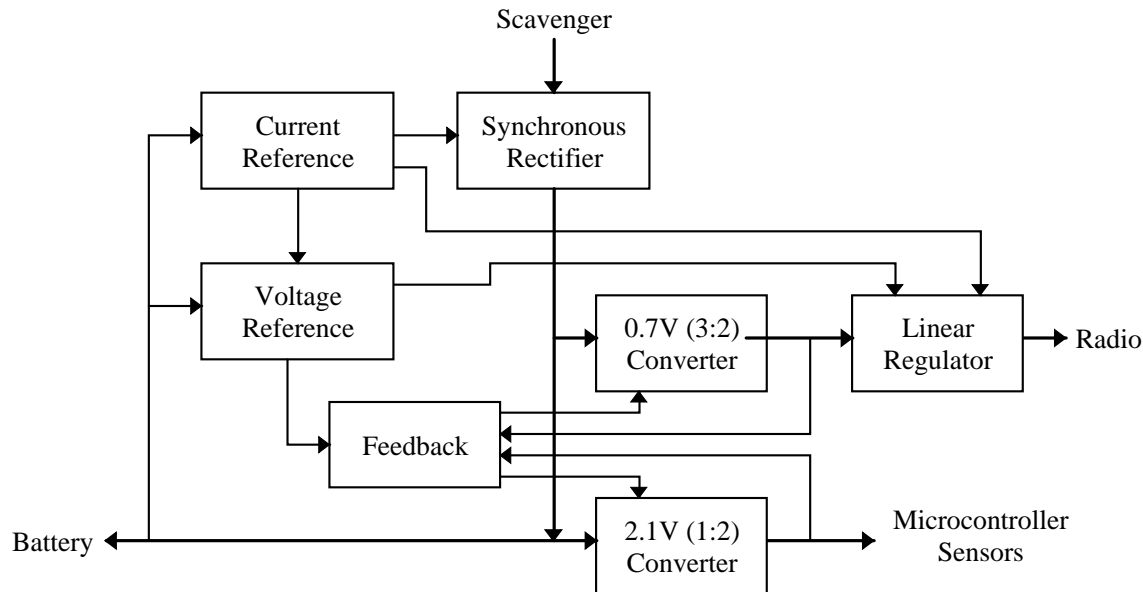


Figure 7.3. Block diagram of the converter IC

stages of these converters is detailed in section 7.2, while the gate drive techniques used are described in section 7.3.

An ultra-low-power linear regulator is used as a post-regulator to more-precisely set the radio supply voltage to 0.65 V and to smooth the ripple from the switched-capacitor converter. This linear regulator is designed with an integrated switch to disable the regulator's output. When the output is disabled, the regulator's bias current is decreased substantially to reduce quiescent power. The enable transistor is located between the output capacitor and the load such that the output capacitor remains charged while the output is disabled. Thus, the energy stored in the capacitor is preserved and the turn-on transient response is shortened. Finally, a hysteretic feedback controller is used to regulate output voltage and switching frequency, and is described in section 7.5.

A number of analog blocks provide support to the power electronics by providing references and control signals. A self-biased current source (reference) supplies bias current to the chip via a current mirror. It is biased at 18 nA independent of V_{DD} and mildly dependent on temperature. An ultra-low-power sampled bandgap reference provides a reference

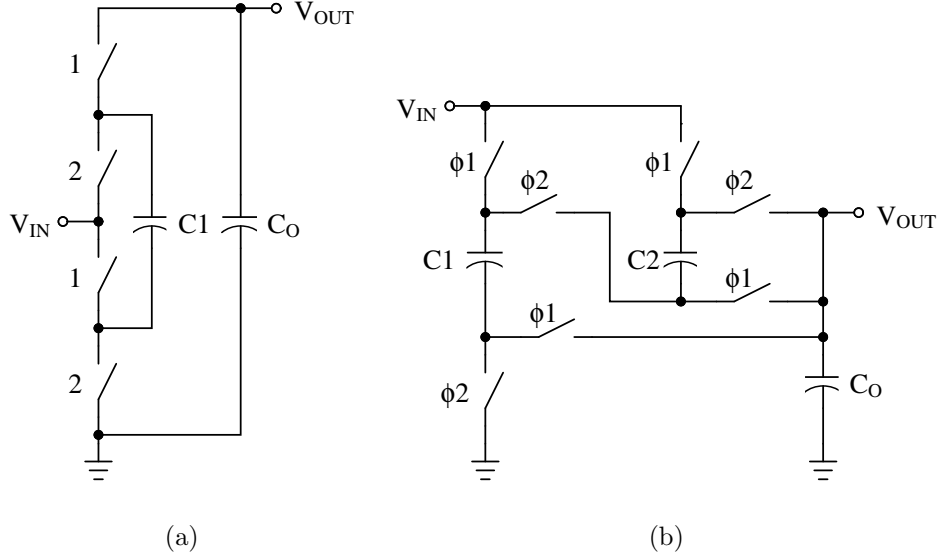


Figure 7.4. Switch-level diagram of a) 1:2 converter, b) 3:2 converter

voltage to both the converter feedback circuitry and the linear regulators. The design of this voltage reference is further described in section 7.5.

The converter IC was implemented using a $0.13\ \mu\text{m}$ CMOS process provided by STMicroelectronics. The nominal 1.2V working voltage matches the battery voltage perfectly, and the process provides $2.5\ \text{V}$ transistors and high-density capacitors, the latter used in the switched-capacitor converters.

7.2 Converter Architecture and Optimization

Two independent switched-capacitor (SC) converters perform the power conversion between the battery and the loads. A 1:2 ratio converter, shown in figure 7.4a, provides a doubled voltage for the microcontroller and sensors. The minimum supply voltage for these components is $2.1\ \text{V}$. A 3:2 ratio converter, shown in figure 7.4b, provides a lower voltage (nominally 0.65V) to supply the radio.

The topologies are chosen to utilize the native transistors of the $0.13\ \mu\text{m}$ CMOS process, even to generate the $2.1\ \text{V}$ rail. The benefits and drawbacks of a number of SC converter

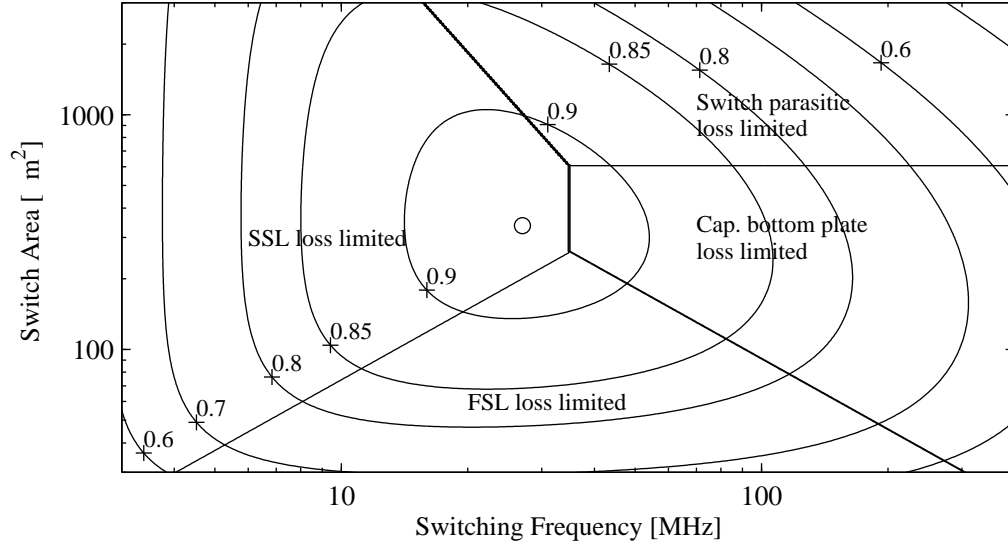
topologies are described in chapter 4. All power switches are implemented using triple-well NMOS transistors to minimize die area and gating and parasitic losses. Section 7.3 addresses the level shifters and other circuitry required to drive these transistors.

The transistors, capacitors and converter switching frequency of each converter are adjusted to optimize efficiency while meeting constraints on output voltage, power and die area. In chapter 3, a method to optimize transistor and capacitor sizes, and the relative allocation of die area between transistors and capacitors, was developed. Those techniques will be applied here to size the various components and choose the maximum switching frequency. Under nominal operating conditions, switching frequency will be regulated via a hysteretic control loop described in section 7.5. The converter is optimized to maximize efficiency via this method while keeping the output impedance sufficiently low such that the required output voltage is maintained at maximum output current. A margin of error for process tolerances needs to be included as well.

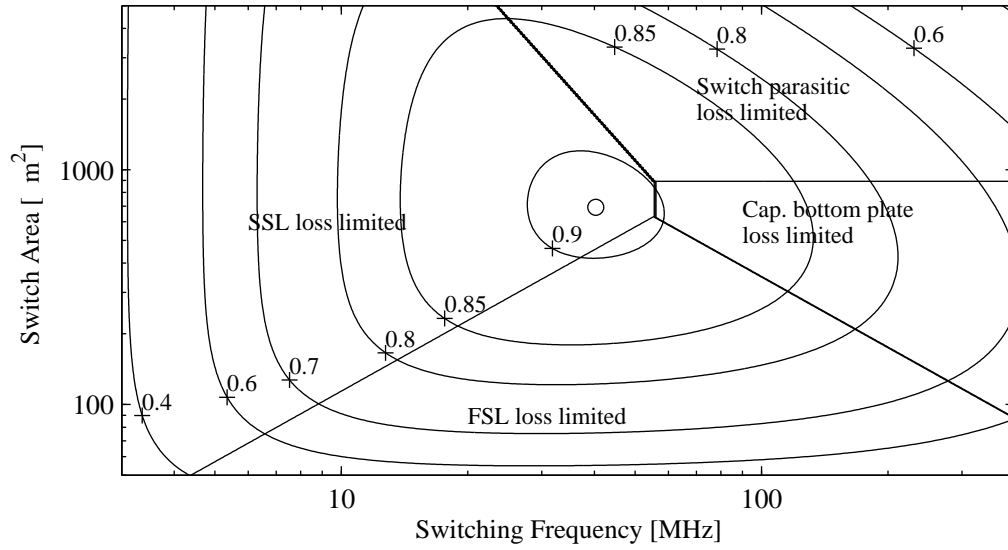
To optimize the SC converters, the total capacitor area is constrained to a prescribed area, and the relative capacitor sizes within each converter are adjusted by the optimization in chapter 3. Metal-insulator-metal (MIM) capacitors are used for all capacitors as they have a relatively-high capacitance density and low bottom-plate parasitic capacitance. Next, the capacitor area is divided between the two converters such that both would run at the same switching frequency (to allow for a single clock), while minimizing net loss. The two remaining variables are the switch area (for each converter) and the switching frequency. A numerical optimization is performed by evaluating efficiency and output impedance over a range of switching frequencies and switch areas.

Figure 7.5 shows contour plots of the converter efficiency swept over switching frequency and switch area for the 1:2 and 3:2 converters. Contour efficiencies are indicated. The optimal design lies in a wide plateau between 90% and 92% efficiency. The solid straight lines separate the space into four regions, indicating where each of the four indicated loss mechanisms are dominant.

The two converters were designed with a slightly higher switching frequency and switch



(a)



(b)

Figure 7.5. Optimization contours of the (a) 1:2 converter and (b) 3:2 converter

area than optimal to ensure the output impedance was sufficiently low across the process corners. A nominal switching frequency of 30 MHz was chosen, along with switch areas of 550 and 950 μm^2 for the 1:2 and 3:2 converters, respectively. The anticipated full-load open-loop efficiencies of these two converters are between 90% and 92% for both the 1:2 and 3:2 converters.

7.3 Gate Drive

Since both converters use only native 0.13 μm NMOS devices, driving the gates is not trivial. Two gate-drive structures have been developed for the two SC converters.

The 1:2 ladder converter exhibits a regular structure that can be extended for higher ratio conversions. This ladder topology can be driven with cascode level-shifters. The cascode level shifters [40] are made with triple-well 0.13 μm devices and can translate a signal up an arbitrary number of levels. This implementation is shown in figure 7.6 for an intermediate stage in a ladder converter.

Each level shifter and its gate driver are powered from the local power capacitor connected to the relevant switch's source. For instance, capacitor C2 in figure 7.6 powers the circuitry to drive M2. A pair of cross-coupled inverters form a latch, regenerating the signals at each stage. Two pull-down signals, connected to the sources of M5 and M8, toggle the latch to either the *on* or *off* position. Two NMOS transistors (M7 and M10) then reproduce these signals to drive the level-shifter above it.

Since all transistors in the level-shifter are 1.2V triple-well devices, shielding devices are needed to prevent device breakdown. Cascode pairs (e.g. M5, M6 and M8, M9) are used to shield both the NMOS pull-down transistor and the gates of the NMOS transistors. The threshold of these cascode devices limit the minimum voltage and speed of the level shifter. Transistor sizing and optimization is critical to ensure operation over rail-voltage variation.

The top transistor in the NMOS transistor stack implementing the ladder converter is driven based on a floating supply. The ladder structure of the power devices is continued

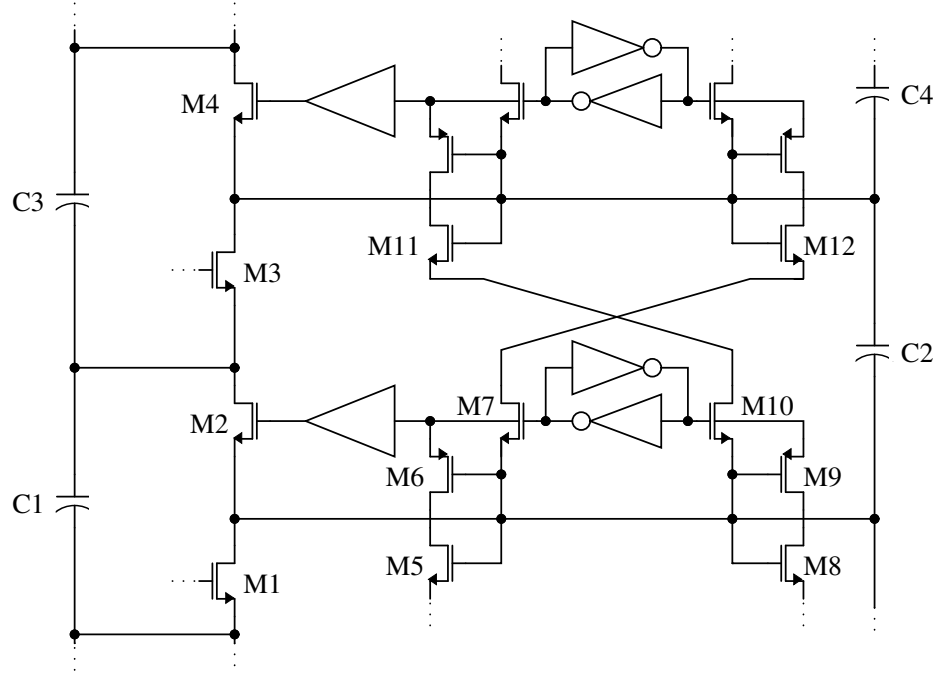


Figure 7.6. Cascode level-shift gate drive for the 1:2 ladder converter

by one or two more smaller transistors, creating higher potentials to drive each of the large power-path switches. The top transistor in the extended ladder is implemented using a PMOS device and driven by the same source as the NMOS transistor beneath it.

An alternate gate drive structure is used for the 3:2 converter. Since the sources of all the transistors in this converter (in figure 7.4b) never exceed the V_{DD} rail, a more-direct drive can be used. This charge-pump gate drive, shown in figure 7.7, uses a flying capacitor charged to the 1.2V supply to directly drive the gate of a transistor with a non-grounded source. In the 3:2 converter, six of the seven transistors are driven this way. The remaining transistor has its source connected to ground, and is driven with an inverter-chain buffer.

The operation of this gate drive circuit will be examined with respect to the drive signal CLK . When CLK is low, the power transistor gate is discharged to ground via transistors M6 and M7. Also, the flying cap C1 is charged to V_{OUT} via M4 and M1.

When CLK is high, C1 charges the gate of the power transistor to $V_{DD} + V_{OUT}$ through

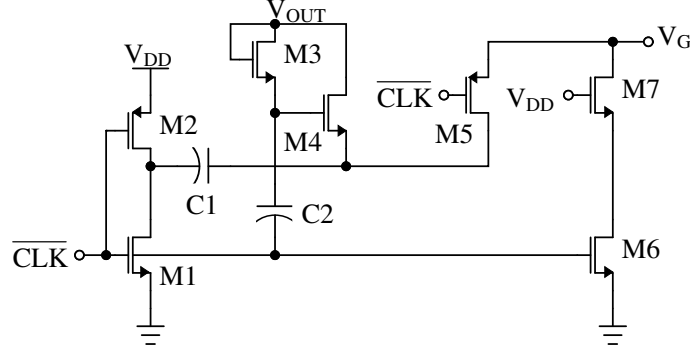


Figure 7.7. Capacitor-boost gate drive for the 3:2 converter

M2 and M5. C1 is the primary capacitor of the charge pump which charges the power capacitor to the appropriate voltage. In addition, assist cap C2 is charged to V_{OUT} via diode-connected M3. Capacitor C2 eliminates the diode drop of M4 while charging C1 when CLK is low.

Capacitor C1 is sized such that it dominates the gate capacitance of the power transistor, enabling the gate to be charged to $V_{DD} + V_{OUT}$. For each of the three gate drive circuits (each driving two switches), a single 2 pF MIM capacitor was used. While in the on-state, these power transistors' sources are at V_{OUT} , so their gates are driven correctly. This gate driver, along with the cascode level-shifter for the 1:2 converter, ensure efficient converter operation using only the native 0.13 μm NMOS devices.

7.4 Synchronous Rectifier

The tire pressure sensor is powered using an electromagnetic shaker. A small permanent magnet moves inside a cylinder wrapped with a multi-turn winding, shown in figure 7.8a. The shaker axis is oriented tangential to the circumference of the wheel. The varying gravitational force in the frame of the rotating wheel causes the magnet to fall back and forth in the cylinder. The local centrifugal force is normal to the direction of magnet travel, creating a normal force depending on the rotation speed. Each time the magnet falls from

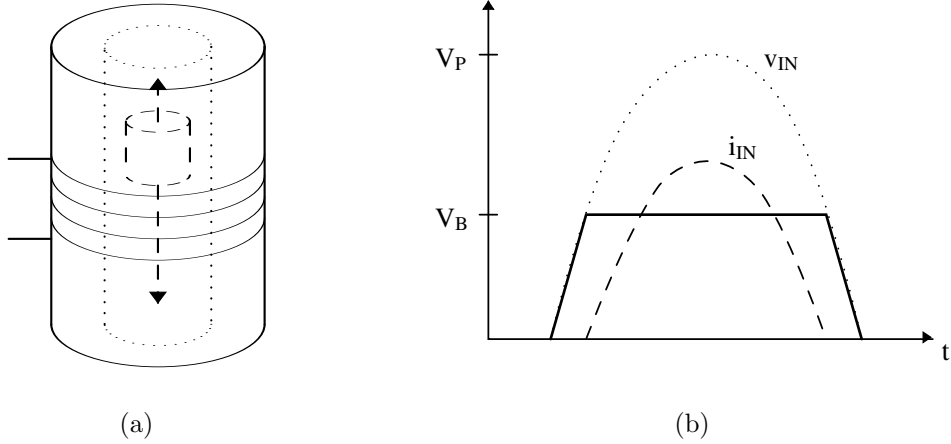


Figure 7.8. Shaker (a) design and (b) example input waveform

one side to another, a pulse of voltage is created. To charge a battery or capacitor, these pulses must be rectified.

Simple diode-based rectifiers are convenient but the forward voltage drop severely impacts efficiency at low system voltages. A synchronous rectifier (see figure 7.9) uses active devices and feedback to perform the rectification function without significant voltage drop and power loss [49, 19, 24, 42]. The synchronous rectifier approaches the efficiency of an ideal diode rectifier. Since the pulse shape and amplitude are predictable by the nature of the application, the source voltage can be matched to the battery or load voltage by simply changing the number of turns in the single shaker winding. The number of turns on our scavenger are optimized by trial and error to achieve the optimal open-circuit amplitude. For this application, the optimal open-circuit amplitude was determined to be 2.5–3.0 V by the method in section 7.4.1.

Figure 7.9 summarizes the circuits used for the synchronous rectifier. The lower two transistors of the bridge are gated complementarily from a hysteretic comparator. Hysteresis prevents oscillation and allows the circuit to reduce bias current at zero input. Since the magnet is usually not moving (as vehicles are usually parked), energy conservation at zero-input is critical. The threshold of the hysteretic comparator is designed to be approximately ± 0.4 V.

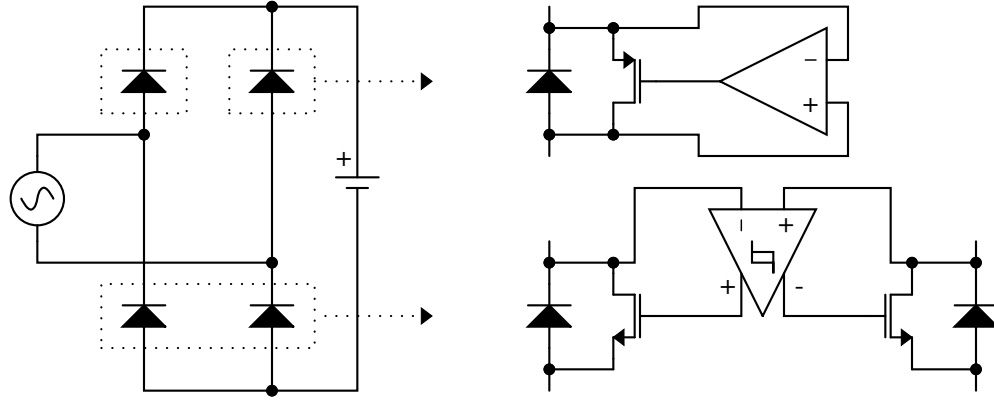


Figure 7.9. Synchronous rectifier circuit

The upper transistors of the bridge run independently and are controlled by comparators continuously sampling the voltage across each of the switches. The delay of the rectifier depends on the bias current and the drain-source voltage difference on the switch. By making the switch large, conduction loss is minimized, but transition time is lengthened. An on-state drop of 20-50 mV and bias current of 10 nA were targeted to achieve a compromise between conduction loss, bias current and delay time. Additionally, a circuit was added to reduce bias current at zero-input conditions, as detailed below.

The circuit used to replace each of the two top-side diodes in the traditional rectifier is shown in figure 7.10a. Transistor M1 is the power transistor which replaces the rectifier diode and is controlled by a two-stage comparator. The body diode of M1 allows for operation as a traditional rectifier when the circuit is powered off. Transistors M2 through M5 and transistors M6 through M9 form the first and second stages of the comparator, respectively. Each stage is driven by a bias current source gated by transistors M10 through M12. These gating transistors are connected to the input voltage, allowing the bias current sources to be shut off when the input voltage falls below the threshold voltage of the transistors. When no mechanical energy is applied to the harvester, the input falls to zero and the quiescent current of the rectifier is greatly reduced. The bias current of the comparator is approximately 4 nA and is reduced when the input is low.

Figure 7.10b shows the implementation of the hysteretic comparator in the synchronous



rectifier design. Transistors M1 and M2 form the power devices which rectify the input signal. Their body diodes can act as standard junction diodes when the circuit is not powered up. Transistors M3 through M6 form a comparator which measures the input voltage and sets the state of the power devices accordingly. Since the devices must switch when the floating input, which is connected to the off-state transistor, swings below ground, the comparator must be designed to allow a negative common-mode voltage at the input. The input devices (M3 and M4) have their sources cross-coupled to allow the sensing of negative voltages, limited by the forward voltage of the body diodes of these transistors. Additionally, when both inputs are at zero volts, the circuit consumes only leakage power because it is essentially a digital circuit.

7.4.1 Impedance matching AC energy harvesters with diode rectifiers

Analysis of a diode rectifier is necessary to compute the optimum number of turns, and thus the optimum peak input voltage, of the electromagnetic harvester. The synchronous rectifier is modeled as an ideal-diode rectifier, since its forward voltage drop is nearly negligible. Figure 7.8b shows a typical waveform for a shaker transition. For simplicity, a single half-period of a sinusoid will be examined. This work assumes constant amplitude sinusoidal pulses, but the method can be extended to arbitrary waveforms. The sinusoidal source, with amplitude V_P and series real impedance R_S , is connected to a battery with voltage V_B through an ideal-diode bridge rectifier. The inductance of the coil does not contribute significantly to the impedance of the harvester at the sub-100-Hz frequency of operation. If the harvester has a natural frequency of ω and pulse repetition frequency of f_{IN} , the open-circuit input voltage over a pulse can be written as:

$$v_{OC}(t) = V_P \cos(\omega t) \quad -\pi/2 \leq \omega t \leq \pi/2. \quad (7.1)$$

When the harvester is connected to the rectifier, the input voltage will be clipped to the battery voltage. A current will flow through the rectifier during a period of time where the

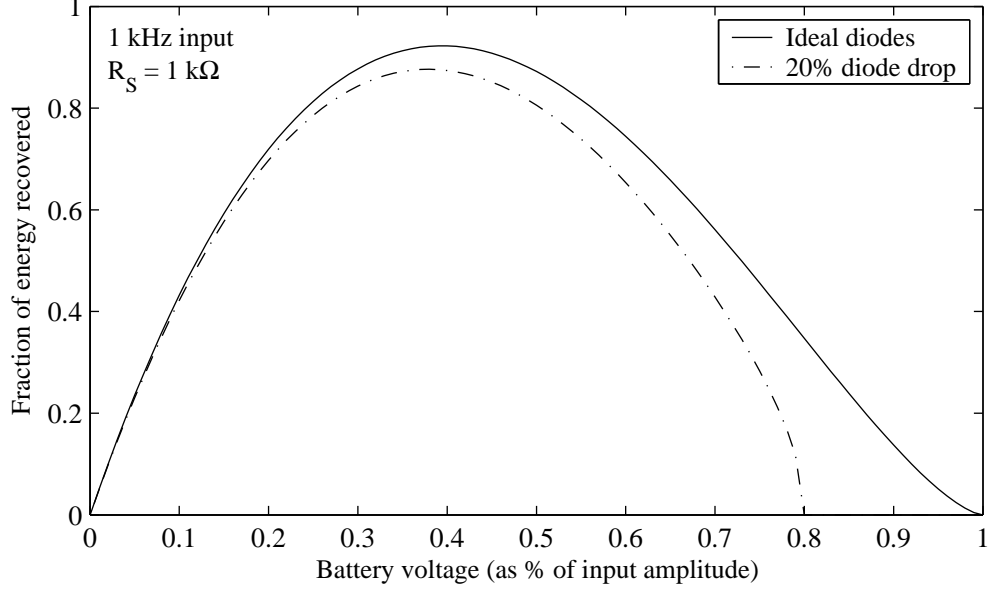


Figure 7.11. Available energy via rectification into a fixed voltage source

open-circuit voltage is greater than the battery voltage in magnitude:

$$-\frac{\cos^{-1}\left(\frac{V_B}{V_P}\right)}{\omega} < t_{ON} < \frac{\cos^{-1}\left(\frac{V_B}{V_P}\right)}{\omega}. \quad (7.2)$$

The current flowing through the rectifier in the on-state can be written as:

$$i_{IN} = \frac{1}{R_S} (V_P \cos(\omega t) - V_B) \quad t \in t_{ON}. \quad (7.3)$$

The energy recovered from a single pulse can be found by integrating the instantaneous power over the conduction angle:

$$E_{IN} = \frac{V_B}{R_S} \int_{-\frac{1}{\omega} \cos^{-1}\left(\frac{V_B}{V_P}\right)}^{\frac{1}{\omega} \cos^{-1}\left(\frac{V_B}{V_P}\right)} (V_P \cos(\omega t) - V_B) dt. \quad (7.4)$$

$$E_{IN} = \frac{2 V_B}{\omega R_S} \left[\sqrt{V_P^2 - V_B^2} - V_B \cos^{-1}\left(\frac{V_B}{V_P}\right) \right]. \quad (7.5)$$

The ideal ratio between V_P and V_B can be found by maximizing E_{IN} with respect to V_B . Figure 7.11 shows the fraction of the available energy harvested plotted as the battery voltage is varied with respect to the input amplitude. This fraction corresponds to the energy obtained from the rectifier divided by the maximum energy available through a

matched resistive load. Additionally, the efficiency is also shown in the case when diodes (each with a drop of 10% of the input amplitude) are used for the rectifier, yielding a 20% loss while charging. The input energy, in (7.5), is compared with the energy obtained from an ideal matched-impedance load. This maximum single-pulse energy is given by:

$$E_{MAX} = \frac{\pi}{\omega} \frac{V_P^2}{8 R_S} \quad (7.6)$$

From this optimization, 93% of the resistively-matched-load energy can be recovered when the peak of the input pulse is approximately 2.5 times the battery voltage. At microwatt power levels, it is not advantageous to pursue the remaining 7% by creating an elaborate impedance-matching circuit. However, if a highly-reactive harvester is used, such as a piezoelectric bender, additional circuitry can be used to extract more energy from the source [42].

7.5 Ultra-Low-Power Analog Circuits

For systems with large peak power to average power ratios, switching frequency control is essential to maintain high efficiencies across operating conditions. Gate drive and other frequency-dependent parasitic loss at the maximum switching frequency is approximately $200 \mu W$ for the converter, which would dominate standby power. To reduce the frequency-dependent power loss, reducing the switching frequency, as the load is reduced, is necessary. Frequency modulation can be used to both reduce the power consumption of the system and to regulate the output voltage of the converter. By keeping the output voltage regulated at the lowest voltage tolerated by the load, load current consumption can be minimized. Regulation is performed on the output voltage of each converter using a hysteretic controller. Hysteretic (thermostat-like) feedback has advantages of being simple to implement and inherently stable for all loads. In addition, hysteretic feedback exhibits near-instant response to large steps in load current, which are common in wireless sensor nodes.

However, hysteretic feedback inherently introduces ripple in the output voltage, which can be filtered by a low-dropout-voltage regulator (LDO) for ripple-intolerant loads. In our

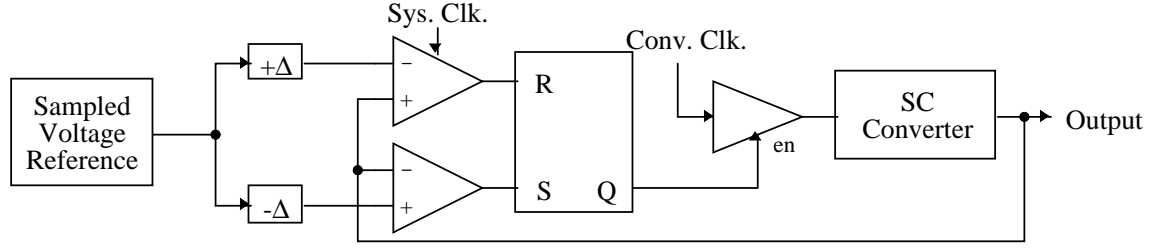


Figure 7.12. Diagram of control logic

application, the radio is sensitive to ripple and variation of its supply, so an LDO is used for post-regulation, dropping an additional 50 mV and reducing ripple by approximately 20 dB.

Figure 7.12 shows the control system. Two clocked comparators [59] compare each converter's output to a pair of reference thresholds every $20 \mu s$. If the output is above the upper threshold, the converter's clock is disabled until the output falls below the lower threshold. The hysteresis zone between the two thresholds causes additional ripple on the output in excess of the ripple discussed in section 5.1.

To bias the analog circuitry on the IC, an ultra-low-power current reference was used. The topology of the reference was chosen to minimize the bias current for a given size resistor. Fig. 7.13a shows the structure of the current reference. The circuit is designed for deep sub-threshold operation, yielding an exponential relation between the drain current and the gate-source voltage. The reference current is set by the resistor R and the voltage drop across it, defined by the difference in gate-source voltage between M1 and M2. The value of this resistor is nominally 500 k Ω . At room temperature, the current reference produces a current of 18 nA, independent of supply voltage. The current reference occupies 0.004 mm² of die area.

A reference voltage is required to perform output voltage regulation. This function is performed by a compact bandgap voltage reference. Even with subthreshold conduction, microamps of current are necessary to allow for sufficiently low process variation. To reduce the average power consumed by this bandgap reference, it was operated at a very low duty

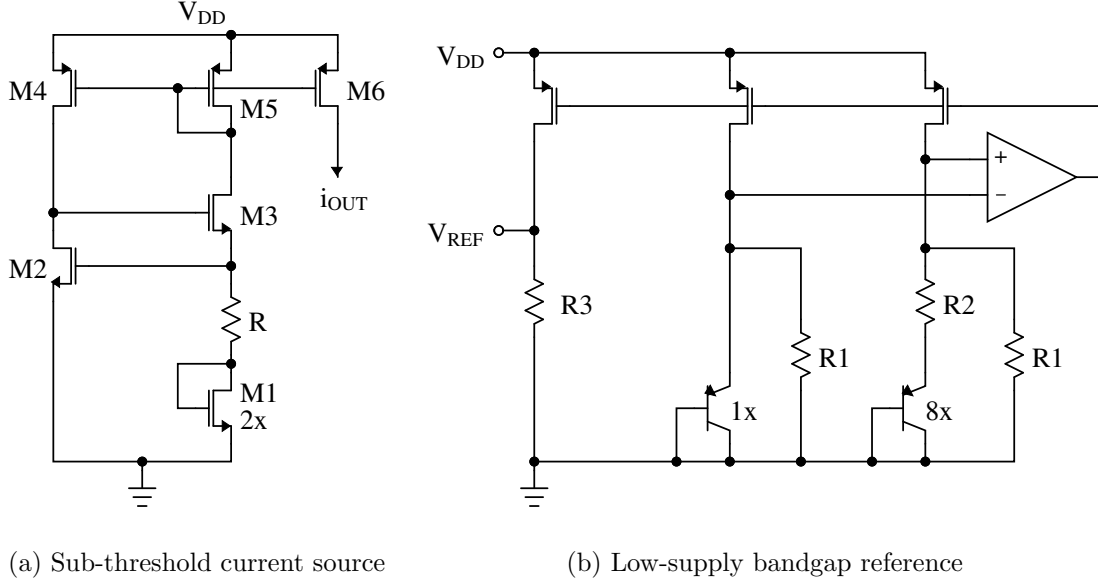


Figure 7.13. Schematics of analog references

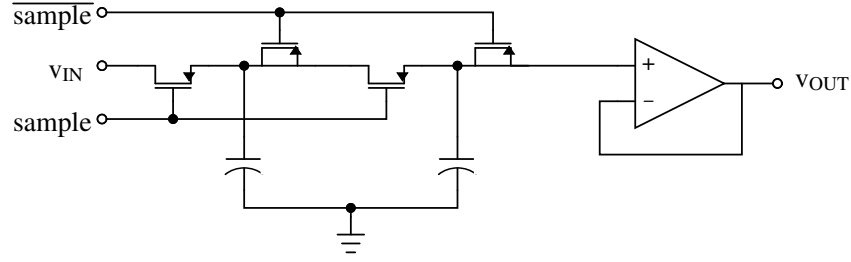


Figure 7.14. Low-leakage sample and hold circuit

cycle and sampled. Since the supply voltage is below the bandgap voltage of silicon (1.2 V), a non-traditional reference structure is used.

The bandgap core (in figure 7.13b) is based on the sub-1V operational circuit presented in [5, 7] with an improved implementation described in [53, 23]. It operates below the bandgap voltage by adding currents, proportional and complementary to absolute temperature (PTAT and CTAT, respectively), instead of voltages. The startup and stabilization of the bandgap circuit was optimized for speed to minimize the duty cycle.

The sample and hold circuit was specifically designed to reduce leakage and charge injection to keep a constant output voltage with a long period between samples. Figure 7.14

shows the two-stage sample and hold circuit. Opposing matched PMOS transistors counter the charge injection from turning off the sampling transistors. Thick-oxide transistors were used for the input of the follower to reduce gate tunneling current, which otherwise becomes significant for small sampling capacitors and long hold times if thin-oxide devices were used. Since the sampling transistors dominate the leakage rate, a two-stage circuit was used. The first sampling capacitor discharges linearly to the input (which is at a low potential when the bandgap reference is off). The second capacitor, discharges based on the difference between the two capacitor voltages, forming a quadratic voltage profile. This sample and hold topology is more space-efficient than a single-stage circuit using a larger capacitor for a given sample rate.

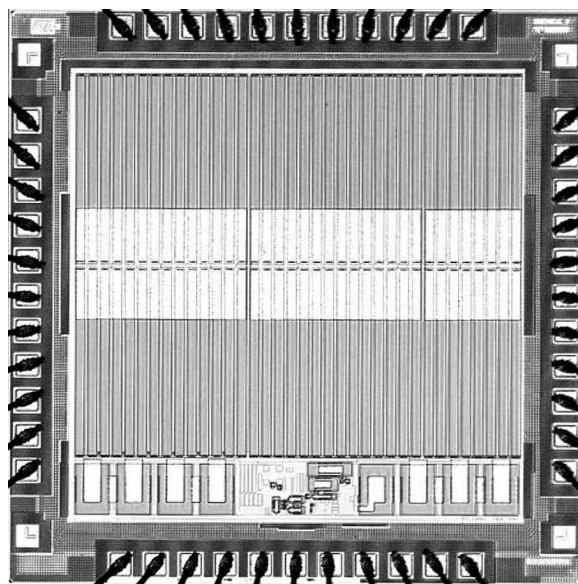


Figure 7.15. Photomicrograph of power interface IC

The IC was fabricated using the STMicroelectronics $0.13\ \mu\text{m}$ CMOS process. The die, shown in figure 7.15, is approximately 2 mm on a side, significantly smaller than discrete, off-the-shelf system implementations. The die area is dominated by the flying capacitors and the pad ring. The analog circuitry and power transistors occupy the $420\ \mu\text{m} \times 200\ \mu\text{m}$ region at the bottom-center of the IC. In this IC, the leakage current was approximately $6.5\ \mu\text{A}$, a combination of analog quiescent current, ESD structure and pad ring leakage, and component leakage.

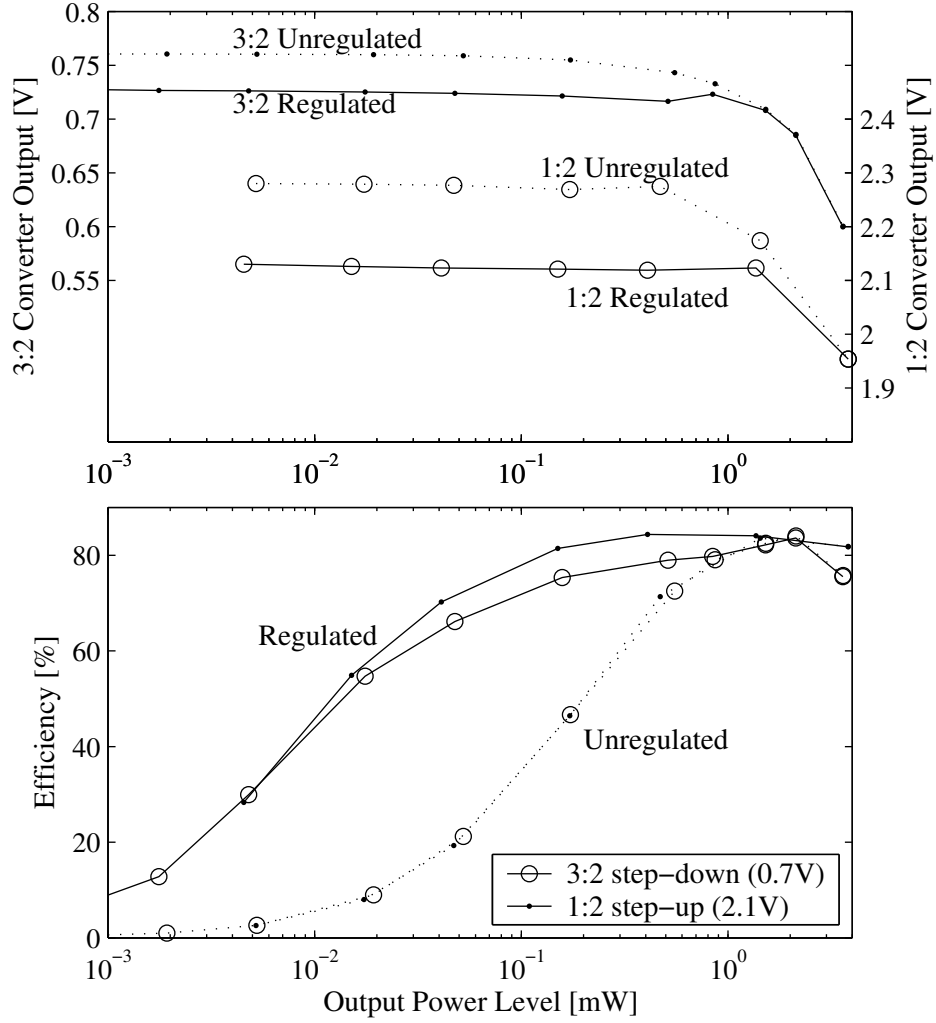


Figure 7.16. SC Converter output voltage and efficiency, $V_{in} = 1.15V$

Both switched-capacitor converters were tested over a range of loads. The output voltage and efficiency of both converters with and without regulation are shown in figure 7.16. The efficiency data include the quiescent current of the chip, so nominal converter-only efficiencies would be higher. The results show that the regulation function works to achieve a constant output voltage and to dramatically improve efficiency at low power levels. When an overload condition causes the output to drop below the regulation level, the output voltage and efficiency are not affected by the feedback, since the converter is continuously operating at maximum switching frequency. The 3:2 converter and 1:2 converter achieve

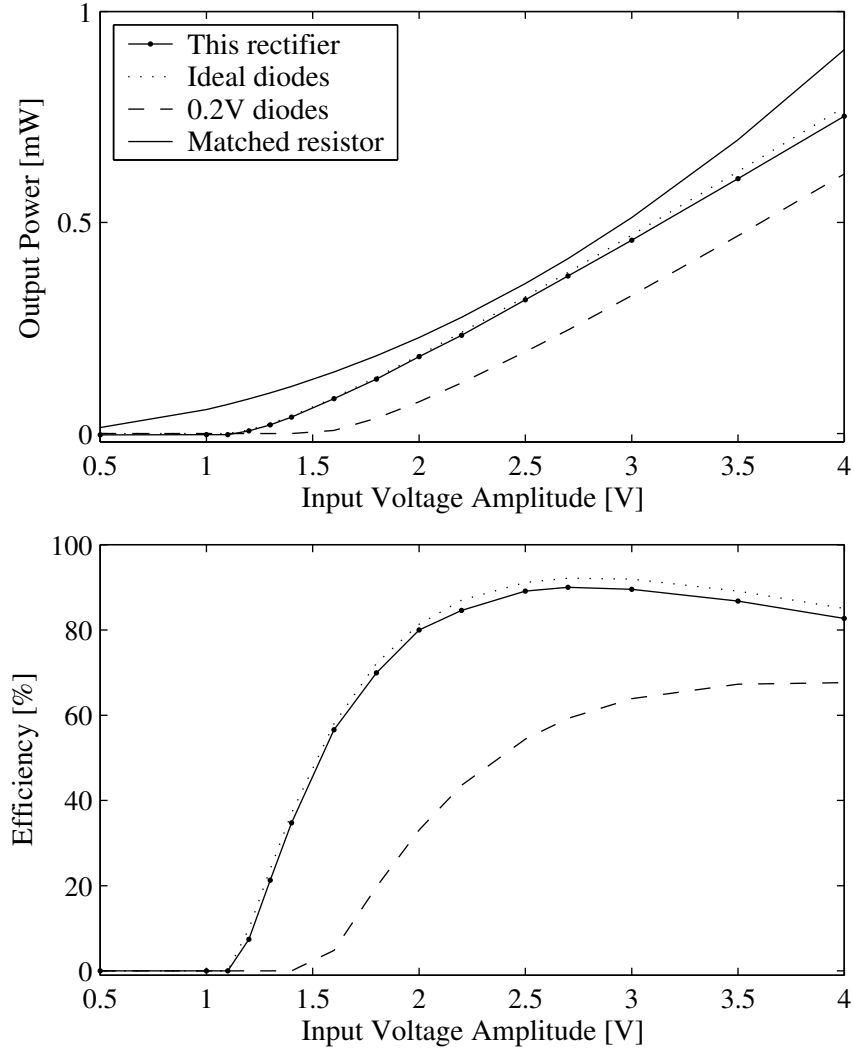


Figure 7.17. Power output and efficiency of synchronous rectifier, $V_B = 1.2V$, $R_S = 2.0k\Omega$, 100 Hz input

peak efficiencies of 83.7% and 84.3%, respectively. Efficiency for both regulated converters remains above 60% for output power levels in a wide range between $20 \mu W$ and $4 mW$.

The performance of the synchronous rectifier is evaluated using a sinusoidal voltage source, with a $2.0 k\Omega$ series resistance, modeling the impedance of the scavenger. The rectifier was compared to three idealized interface models: an exact impedance match ($2.0 k\Omega$ load resistor), an ideal diode rectifier into a fixed voltage source, and a diode bridge rectifier with a forward voltage of 0.2 volts per diode. The third interface represents a Schottky-based diode bridge rectifier, typical of an off-the-shelf implementation.

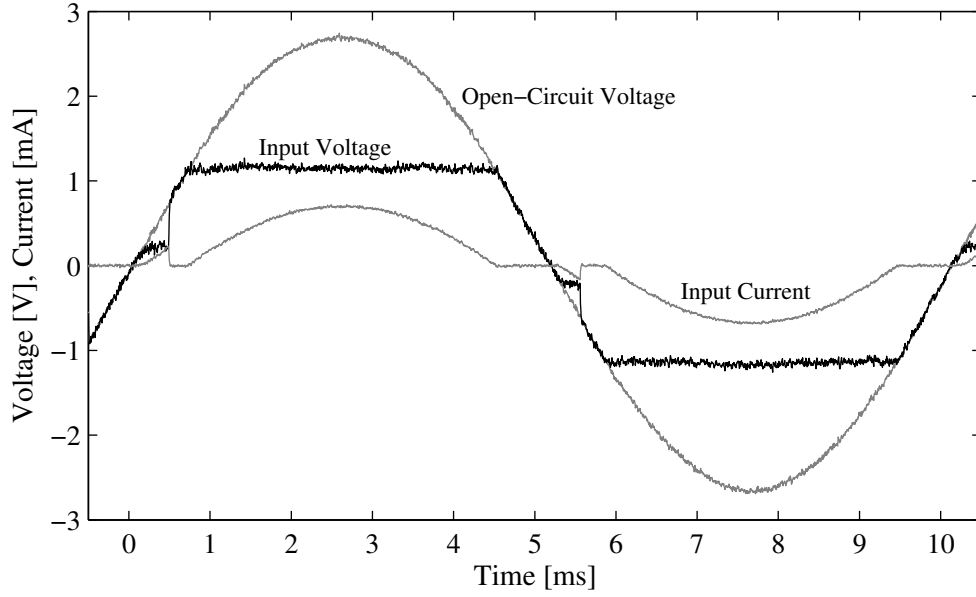


Figure 7.18. Synchronous rectifier waveforms (at 100 Hz)

The efficiency and output power of the synchronous rectifier, and the idealized rectifiers, are plotted in figure 7.17. A battery voltage of 1.2 V was used. Results were identical at 100 Hz and 1 kHz input frequency, and both measured data were nearly identical to the performance of the ideal rectifier. The frequency range below 1 kHz includes this scavenger and the majority of available vibrational scavengers[45]. The peak efficiency of 88%, relative to the matched-impedance case, is obtained at an input amplitude of 2.7 V. At 10 kHz input, the peak efficiency drops by 10%, due to delay-associated losses. Figure 7.18 shows the voltage and current waveforms of the rectifier with a 100 Hz sinusoidal input. At this frequency, typical of the shaker output, the comparator delays are not noticeable, yielding maximum efficiency.

Compared with the ideal diode rectifier (the practical maximum efficiency), the rectifier obtains a relative efficiency of 95.8%. Of this 4% overall loss, 35% can be attributed to chip-wide quiescent current and 65% to rectifier conduction loss and switching delay. The synchronous rectifier has been shown to be significantly more efficient than a diode-based rectifier, and to approach ideal behavior.

Operation	Load Power	Source Power	Time/cycle	Energy/cycle	Efficiency
Standby	0.5 μ W	8.6 μ W	5.98 s	51.5 μ J	5.8%
Wakeup	1.4 mW	1.67 mW	2.5 ms	4.18 μ J	84%
Sensing	450 μ W	540 μ W	6 ms	3.24 μ J	84%
Transmission	2.5 mW	3.0 mW	5.5 ms	16.5 μ J	84%
Average	6.0 μ W	12.57 μ W	6.0 s	75.42 μ J	47.7%

Table 7.1. Energy efficiency over sensing period

7.6 System Efficiency

Since the PicoCube operates in numerous power modes, calculating the average power consumption is important in sizing the scavenger and determining necessary input energy. In battery-operated systems, this average power consumption determines battery lifetime. Additionally, by finding the mode with the largest energy consumption, improvements can be made where they are most useful.

The PicoCube power conversion IC was tested at all the load conditions in figure 7.2. Standby power was tested at the smallest load power available, as shown in figure 7.16. The efficiencies in each of these modes are shown in table 7.1. Over the six-second period, the sensor consumes 75.42 μ J, 68% of which is consumed during idle. While the system efficiency of 47.7% is reasonable for such an application, further improvement of the standby power would greatly improve the efficiency. At the target standby power of 1 μ W, the overall system efficiency would improve to approximately 75 %. Since the ESD pad ring on this IC consumed approximately 2.5 μ W, to achieve an ultra-low standby power, a design with the processor, radio, sensors and power processing circuitry on a single design would be necessary.

Chapter 8

Switched-Capacitor Converters for Microprocessors

Switched-capacitor (SC) converters have been used for many low-power applications. Chapter 7 discussed the use of SC converters for ultra-low-power wireless sensor nodes. However, using the design and optimization methods in chapters 2 and 3 and modern CMOS processes, the power density of SC converters can be increased. This chapter describes the feasibility and use of SC converters for high-power-density microprocessor applications.

Microprocessors have always been constructed using the most modern IC technologies. While clock speeds and computational power per watt has been steadily increasing, the supply power recently reached a practical limit imposed by thermal and economic constraints. Supply voltage has become lower with each new generation while supply currents have increased to keep power constant. This trend has placed severe limits on the design of voltage regulators (VRs). The number of pins on modern microprocessors devoted to power is in the hundreds, often two-thirds of the total number of pins [46, 17, 54]. To power numerous power domains on a microprocessor, numerous power rails are required, dividing up the power pins and package power planes, yielding an inherent design inefficiency.

Furthermore, the modern multi-core trend has worsened this requirement, as each core

can be in a different sleep state. If each core requires a different supply voltage, based on its sleep state, the number of input rails becomes unmanageable. For multi-core microprocessors, having a single input voltage and on-die power converters to supply each core becomes highly desirable. Switched-capacitor (SC) DC-DC converters are ideal for on-die power conversion as they can be highly efficient even at high power densities and require no off-chip components, such as inductors.

Inductor-based buck converters have been investigated for this application, using on-die inductors [16, 22] and in-package inductors [47, 20]. However, the on-die inductors require a very specialized custom processing step and the converters made with them still have poor efficiencies. The in-package inductor buck converters are efficient, but require magnetics in package, which requires significant chip metal and I/O usage. This metal and I/O usage increases the series resistance of a converter, decreasing its efficiency. An on-die SC converter requires no specialized processing steps and does not increase I/O utilization. Using a standard-cell-based design, as discussed in section 8.2.2, the ESR can be minimized, resulting in a highly-efficient converter.

8.1 Power Density vs. Scaling

As CMOS technology has progressed, transistors have improved their performance by increasing the ratio of conductance to gate capacitance (i.e. the f_T of a transistor). Similarly, equivalent oxide thicknesses have shrunk, resulting in denser on-chip capacitors. Combining these factors, the power density limit of SC converters has increased with the reduction of feature size. Using parameters from the ITRS roadmap [1] from 2003 and 2007, estimated circuit parameters can be found for numerous process generations. Table 8.1 shows the relevant parameters for the 90nm through 16nm technology nodes.

These parameters can be used to make idealized device models as used in the analysis methods developed in chapters 2 through 4. These models can then be used to evaluate the performance of an SC converter using each of these technology nodes. In figure 8.1,

Technology Node:	90 nm	65 nm	45 nm	32 nm	22 nm	16 nm
Equiv. Oxide Thick. [nm]	1.2	1.0	0.9	0.55	0.5	0.4
Gate Leakage [A/cm ²]	450	600	909	1250	1820	2500
V _{DD} [V]	1.2	1.1	1.0	0.95	0.9	0.7
V _{TH} [mV]	200	150	94	101	99	109
I _{D,leak} [μ A/ μ m] ¹	0.05	0.2	0.71	0.74	0.55	0.48
I _{D,on} [μ A/ μ m] ¹	1110	1300	1510	1820	2245	2535
C _{G,total} [fF/ μ m] ¹	1.0	0.9	0.84	0.8	0.58	0.48

¹per micron width of a minimum-length transistor

Table 8.1. Process parameters from the ITRS roadmap

	TDP	Die Area	Power Density	Total Pins	Power Pins
	[W]	[mm ²]	[W/mm ²]		
65nm Merom [46]	35–80 W	143	0.24–0.56	780 (478)	555 (288)
45nm Atom [17]	0.6 – 2 W	25	0.08	441	
65nm Itanium [54]	170 W	700	0.24		

Table 8.2. TDP and pin counts for three modern Intel microprocessors

the performance of a 2:1 doubler converter is compared in two ways. First, the efficiency of the converter is compared if the power density is held constant at 1 W/mm². Second, the power density of the converter when scaled is examined if efficiency is held constant at 85%. In both cases, the output voltage is scaled to match that of the process.

As the power density of SC converters improves with scaling, the die area expansion required for on-die power conversion becomes minimal. Converter efficiency must be held high such that performance does not decrease significantly to keep total die power dissipation constant. Using on-die power converters, the number of power pins for a microprocessor can be greatly decreased. Table 8.2 shows a number of modern microprocessors, including their thermal design points (TDPs) in terms of die area and the number of supply pins used.

The number of pins assigned to the power interface is dominant in the 65nm Core 2

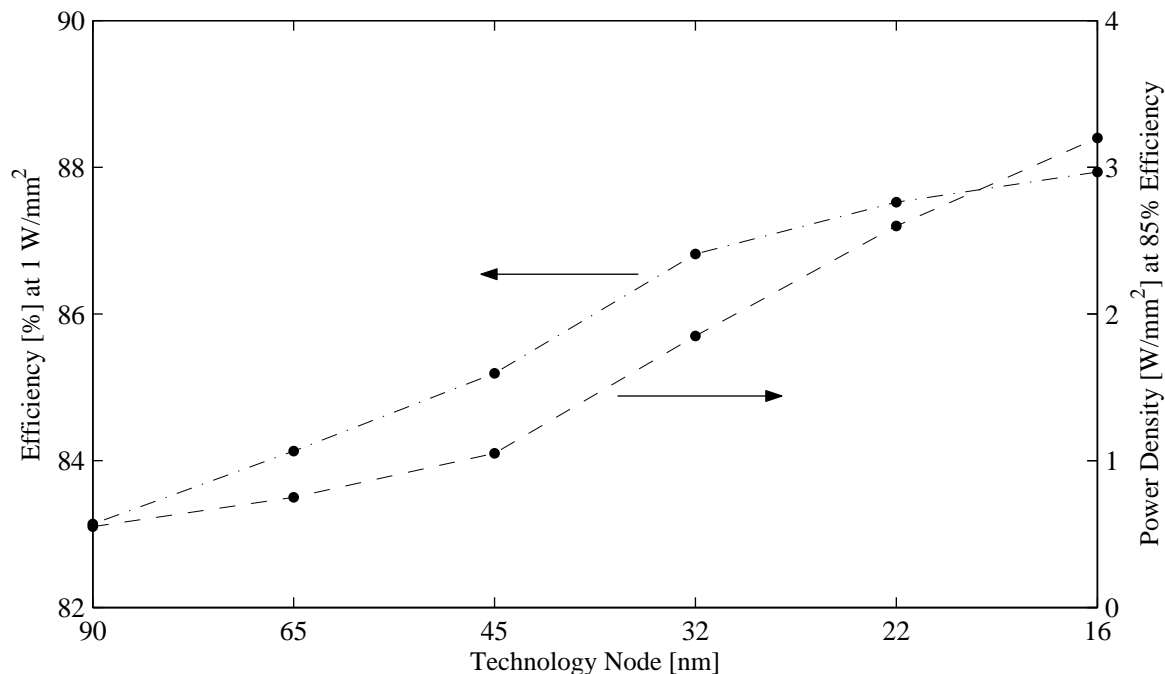


Figure 8.1. SC converter performance versus ITRS technology node

Duo (Merom) processor, the consumer-grade Intel microprocessor. In future multi-core processors, use of on-chip SC converters will enable great reduction in the number of power pins while only modestly increasing die area and TDP. If an 85% efficient converter is used to power a 32nm mobile version of the Merom, the die area would increase approximately 13% and the design power would increase from 35W to 42W. If MIM capacitors are used, the die area may not increase and efficiency can be further improved, since the capacitors can be built on top of the processor's transistors.

8.2 Converter Design

The topology proposed for this application is the triple-ratio, nine-switch topology shown in figure 8.2a [27]. By varying how the switches are clocked, according to figure 8.2b, conversion ratios of 3:2, 2:1 and 3:1 can be obtained. With a 1.8 V input, nominal output voltages of 1.2, 0.9 and 0.6 V can be independently obtained. When the converter's output impedance is considered, these three output voltages drop to approximately 1.05,

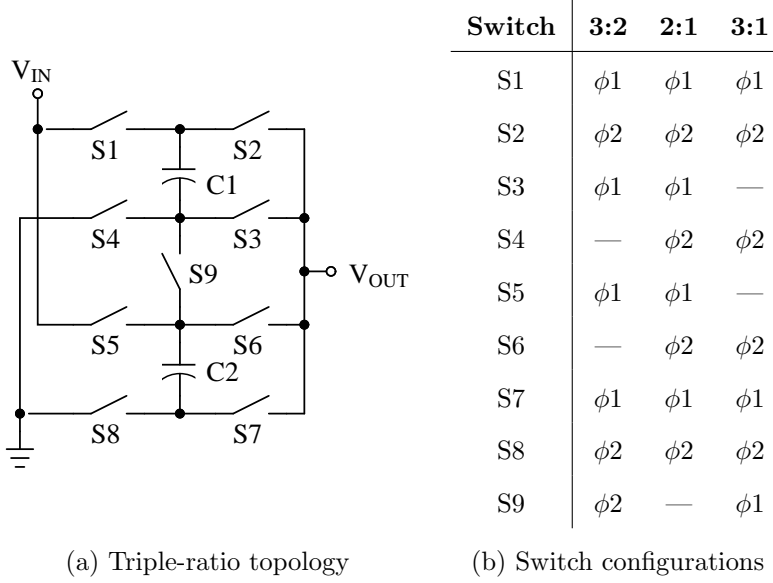


Figure 8.2. Triple-ratio topology and its switch configurations

0.8 and 0.5 volts, respectively. These three voltages can be used to supply a microprocessor in full-speed active, low-speed active and standby modes, respectively. By operating the microprocessor at one of the three optimal voltages, maximum efficiency can be obtained.

This topology will be evaluated for a 1 W/mm^2 application using the 32nm CMOS process using ITRS-based estimated parameters. The PMOS-based flying capacitors are created using the native oxide thickness and an approximate bottom-plate capacitance ratio of 0.75%.¹ The power density of the converter is 1 W/mm^2 at the 1.05 V design point (with a 1.8 V input). Figure 8.3 shows the efficiency of the triple-ratio converter across a range of output voltages for both a resistive load and a ring-oscillator load. With the resistive load, output current scales proportionally with output voltage such that the output power density at 1.05 V is equal to 1 W. Similarly, the ring oscillator exhibits a current-voltage relationship as derived in section 8.2.1.

The converter achieves greater than 80% efficiency at the two primary operating points (1.05 V and 0.8 V), as shown in figure 8.3. Using the ring-oscillator load model, efficiency at low powers increase because the supply current is reduced significantly over the resistive

¹This value may be optimistically low. The optimization of the bottom-plate capacitance of PMOS-based oxide capacitors is discussed in section 8.3.3.

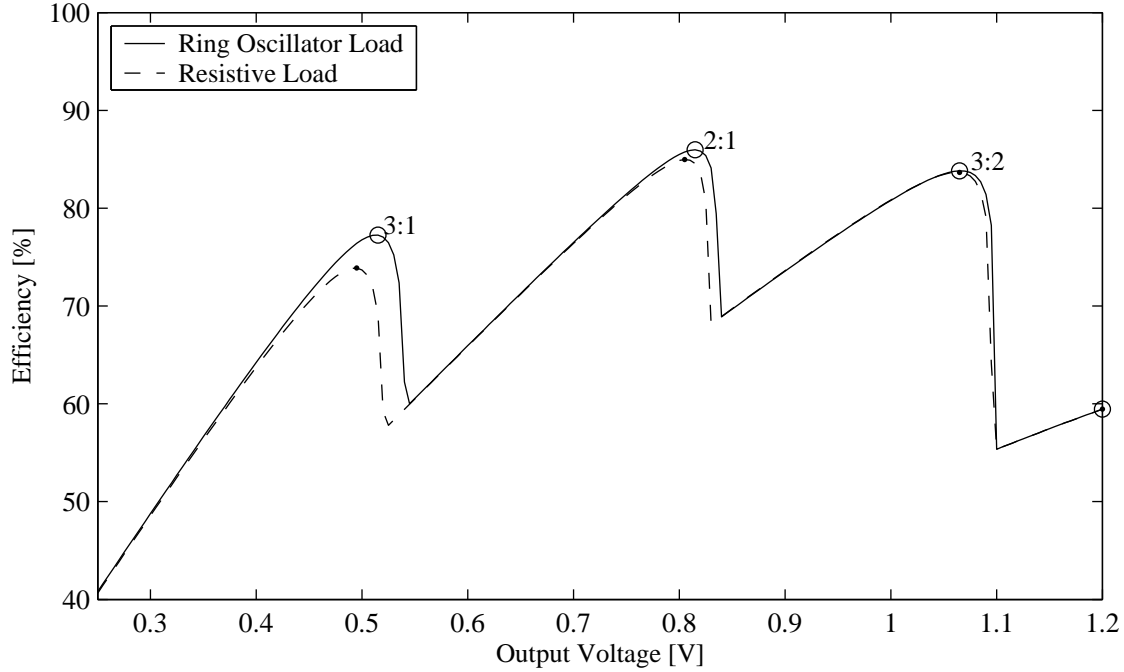


Figure 8.3. Efficiency plot of triple-ratio topology in a 32nm process

load case. However, since the higher-conversion-ratio topologies are inherently less efficient than the 3:2 topology, the 3:1 design point exhibits a lower conversion efficiency. If processor operation is constrained to the optimal design points, the highest power efficiency can be maintained.

8.2.1 Dynamic Voltage Scaling Analysis

To examine the efficiency and performance of an SC converter for microprocessors, the performance of digital circuits as supply voltage varies should be examined. Previous work explains the advantage of dynamic voltage scaling (DVS) [9] and shows a converter to achieve DVS for an ultra-low-power processor [41]. A 31-stage ring oscillator will be considered as a representative digital circuit to consider the effects of voltage scaling on both frequency and power consumption. These relationships will be derived from fundamentals and will be evaluated using the 32nm ITRS process node.

First, the approximate frequency of a ring oscillator will be found. The time constant

associated with each inverter is related to the product between on-state resistance and input capacitance:

$$\tau = C_{GS}R_{ON} = \frac{C_{G,total}(1 + W_P/W_N)}{G_{D,on}((V_{DD} - V_{TH})/(V_{NOM} - V_{TH}))} \quad (8.1)$$

where V_{NOM} is the gate voltage of the transistor at its full conductance, given by $G_{D,on}$. The gate capacitance is increased by the ratio of the width of the PMOS transistor to the NMOS transistor. Since deep sub-micron devices are compared, the transistor's conductance is scaled by the overdrive voltage, given by the ratio in the denominator of (8.1). If the switching point of the inverter is half the supply, the propagation delay of an inverter can be represented as:

$$t_{pd} = \ln(2) \frac{C_{G,total}(1 + W_P/W_N)}{G_{D,on}((V_{DD} - V_{TH})/(V_{NOM} - V_{TH}))}. \quad (8.2)$$

The frequency of the ring oscillator can be easily found from (8.2):

$$f_{OSC} = \frac{G_{D,on}((V_{DD} - V_{TH})/(V_{NOM} - V_{TH}))}{N \ln(2) C_{G,total}(1 + W_P/W_N)} \propto \frac{V_{DD} - V_{TH}}{V_{NOM} - V_{TH}} \quad (8.3)$$

where N is the number of stages in the oscillator. The proportionality shows the normalized switching frequency of the oscillator as it varies with supply voltage.

Now that oscillator frequency has been derived, an estimate of power consumption can easily be determined. Since the gate capacitance is fully charged and discharged each period, the power consumption of each gate can be written as:

$$P_{INV} = f_{OSC} C_{G,total}(1 + W_P/W_N) V_{DD}^2 + V_{DD} I_{D,Leak} \quad (8.4)$$

where $I_{D,leak}$ is the leakage power of a single inverter. The total power consumption of the inverter can be found by multiplying (8.4) by the number of inverters in the chain. Next, (8.3) is substituted to find the normalized relation between power consumption and supply power:

$$P_{VDD} = N (f_{OSC} C_{G,total}(1 + W_P/W_N) V_{DD}^2 + V_{DD} I_{D,Leak}). \quad (8.5)$$

The relations in (8.3) and (8.5) can be evaluated to calculate the normalized frequency, power consumption and energy per operation as the supply voltage varies. These three

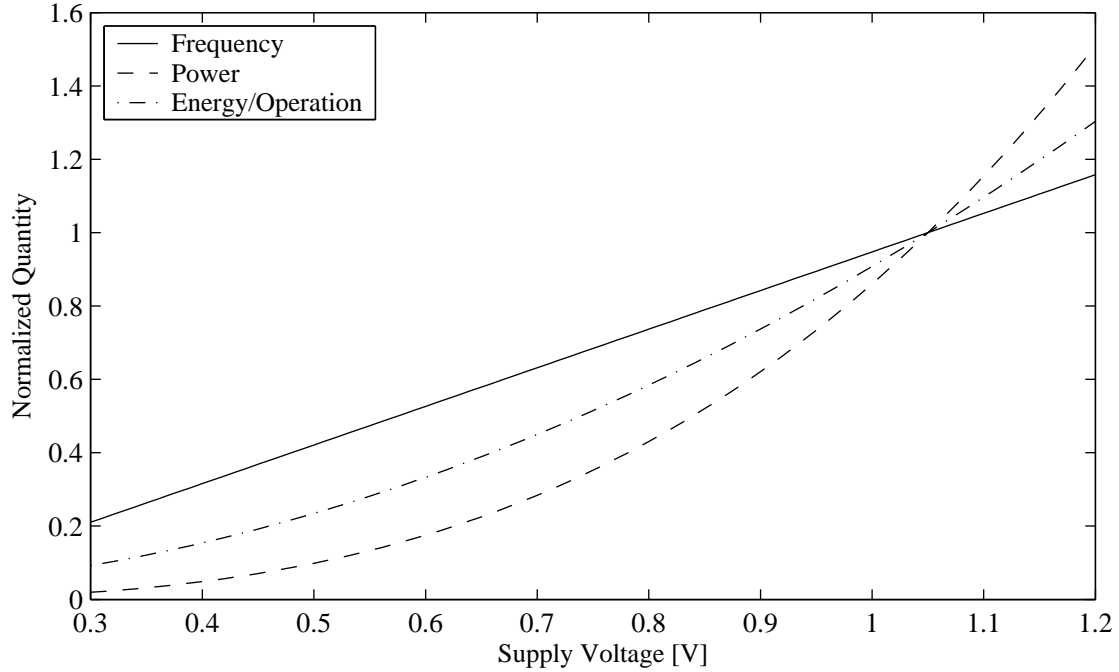


Figure 8.4. Approximate ring oscillator performance versus supply voltage

quantities are compared in figure 8.4. Frequency varies approximately linearly with supply voltage while the power consumption varies approximately by the cube of supply voltage. Thus, the energy per operation of a typical digital circuit varies quadratically with supply voltage. In typical digital circuits, most switches do not switch as fast as the clock, so the ratio of leakage to switching power will be higher than in this model.

Since energy per operation (or Watts per MIPS) is the most important figure of merit for power-limited microprocessors, it is informative to examine the energy per operation of the processor model with and without the use of an SC converter. Figure 8.5 shows the normalized energy per operation of the ring oscillator model by itself, with the SC converter and with an ideal linear regulator supplied from 1.8V. While the SC converter increases the energy per operation of the converter, due to its power loss, three efficient points can be identified (shown by circles). These three points represent peak converter efficiencies and good solutions to the tradeoff between clock frequency and instruction energy. The SC

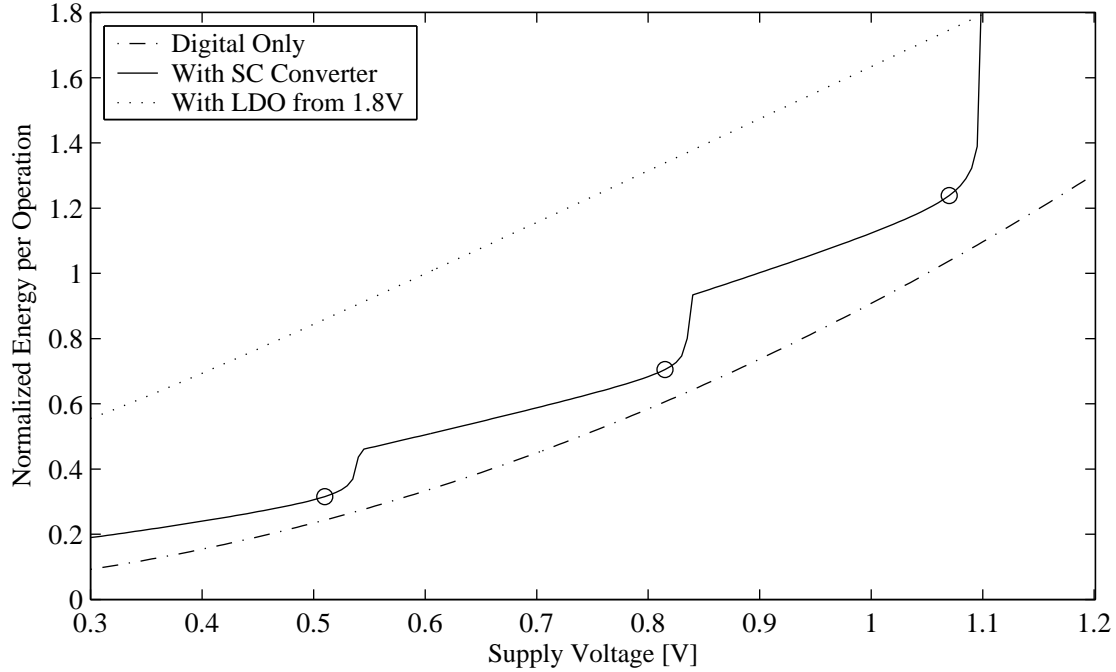


Figure 8.5. Energy per operation using an SC converter

converter provides a substantial improvement in performance over a linear regulator while operating at these three efficient points.

8.2.2 Cell design

The SC converter designed so far in this chapter has not been designed for any specific power. The idealized model, as used so far, takes only power density (i.e. output power divided by die area) into consideration when determining efficiency. While a single converter can be made of any size, there exists an optimal size for each interleaved phase, denoted a *cell*. Each cell implements the topology shown in figure 8.2. Any number of these standard cells can be interleaved to provide the necessary load power while reducing output voltage ripple. Ripple and high-frequency noise can also be reduced by using a high-speed parallel linear regulator [3, 2]. By carefully designing and optimizing a standard converter cell, designing a multiple-rail power distribution network is made significantly easier and more flexible.

The converter cell size (and power level) is constrained by the loss factors that do not scale directly with cell size. If a cell has a particular optimized layout, increasing or decreasing the cell size represents a near-perfect dimensional scaling of the layout. Thus, the number of metal squares used in the layout remains the same regardless of cell size. Thus, the equivalent series resistance (ESR) of the metal used in any sized converter cell is roughly constant. This constant resistance produces a loss which is proportional to the square of output current, motivating the smallest practical cell size.

The second constraint on cell size is the control circuitry needed in any cell which does not scale with cell size. Level shifters and any cell-based control logic fall into this category. As the power level of the cell decreases, this constant control power becomes a more-significant portion of the total power loss. To determine the optimal size of a converter cell, these two loss factors will have to be considered.

To consider the effect of metal ESR, an estimate of metal resistance must be performed. Through a careful layout, using careful design technique, a low-resistance layout can be made. For purposes of illustration, a constant number of metal squares will be arbitrarily assigned to each switch, capacitor and power rail. These numbers would ideally be extracted from the layout of a standard cell in a real design. Each switch is typically designed to have multiple fingers such that it would contribute approximately one square of metal to the layout. A similar design methodology is carried out with the capacitors, also yielding one metal square each. The resistance contribution due to the power rails is less obvious, so 1.5 squares of metal will be assigned to both the input and ground rails, and two squares will be assigned to the output rail.

Next, each of these resistance contributions must be weighted by the square of the appropriate charge multiplier to get the equivalent resistance in terms of the output current. When the 8-switch, 2-capacitor 2:1 conversion ratio case is considered, each switch and capacitor resistance sees a charge multiplier of one-quarter, effectively dividing each resistance by a factor of sixteen. The output rail resistance is not divided at all, while

the resistances of the input and ground rails are divided by a factor of four. Adding these weighted components yields 3.375 equivalent squares of metal.

Since the upper metal layers of a process are often thicker (and have a larger pitch), they should be used for current carrying. A sheet resistance of 25 $m\Omega$ per square will be used, typical of an upper metal layer in a modern process. Thus, the equivalent output-referred ESR of this converter is approximately 85 $m\Omega$. This resistance remains approximately constant regardless of the size of the cell. The loss associated with this resistance can be simply calculated by:

$$P_{ESR} = R_{eq} I_{OUT}^2. \quad (8.6)$$

The second size-constraining loss is the control and level-shifting circuitry. This loss is primarily proportional to switching frequency, so one must assume a nominal operating frequency, typically close to the maximum switching frequency. The maximum switching frequency can be obtained through the numerical optimization in section 3.3.2. In this example, a switching frequency of 400 MHz will be considered, which is the typical full-load switching frequency of this converter designed for a power density of 1 W/mm² using a 32 nm process.

In an example level-shifting circuit, the total transistor width is 8 μm per driver circuit, yielding a total level-shifter capacitance of approximately 120 fF. At a nominal frequency of 400 MHz, the power associated with the level shifter is approximately 48 μW , independent of cell size.

To find the optimal cell size, the power loss associated with these two elements, as a percentage of output power, should be optimized. The full-power case will be used: a 3:2 converter with an output voltage of 1.05 V and a power density of 1 W/mm². Figure 8.6 shows the relation between these two losses and the output power over a range of cell size. For these specific resistive and control losses, the optimal cell size is approximately 0.025 mm², handling 25 mW. At this optimal cell size, the total size-dependent loss subtracts less than 1% from the total system efficiency, and the optimum region is fairly broad. The optimal cell power of 25 mW is very practical from an implementation standpoint and will

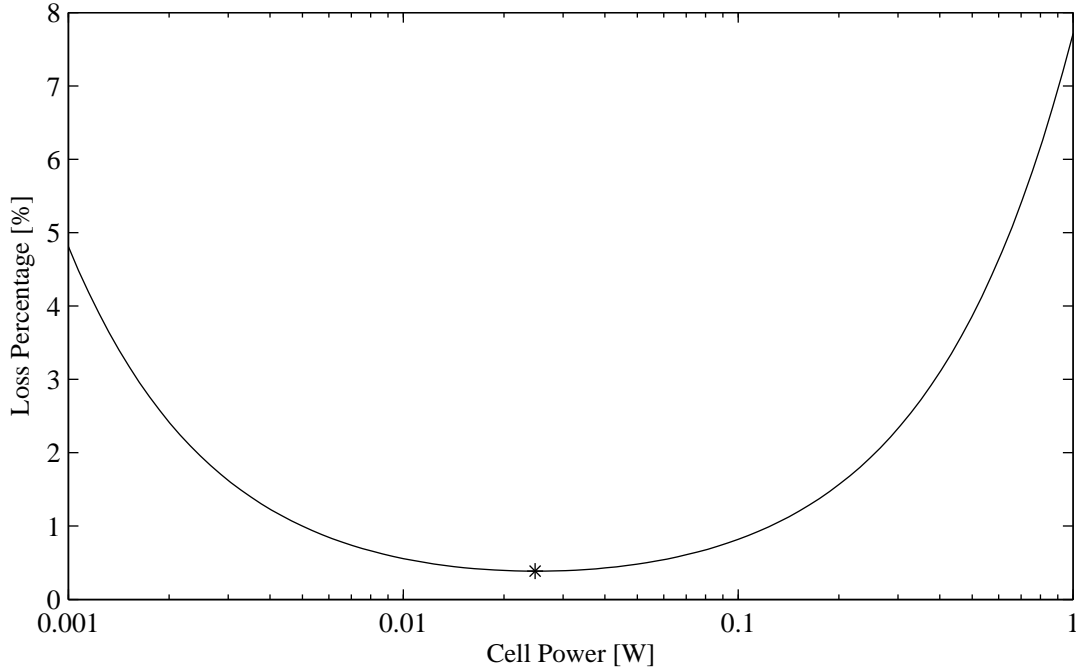


Figure 8.6. Non-scaling components of power loss versus cell size

allow the efficient powering of low-power rails. For higher-power rails, these converters can be distributed around the die to reduce distribution losses and spread the heat dissipation around the die. Also, each cell can function as an interleaved phase in a higher-power multi-phase converter, which will reduce output ripple and the size requirement of the output capacitance.

8.3 Efficiency Improvements

If conversion efficiency is a higher priority than power density or other metrics, additional techniques can be used to improve the efficiency past that calculated in section 8.1 and chapter 3. While the SSL and FSL output impedance losses are direct functions of the component sizing and process parameters, the parasitic-based losses can be reduced through additional design considerations. If parasitic losses are reduced, the converter can be re-optimized around the reduced losses, resulting in a new optimized, more-efficient converter. First, methods of recycling charge from both the transistors' gate and drain parasitic

capacitances will be discussed, followed by methods to reduce the bottom-plate capacitance of MOS capacitors.

8.3.1 Resonant Gate Drive

The gate drive loss comprises the majority of the switch-related parasitic loss of any SC converter. With fully-integrated converters, this loss could represent 20-35% of the loss of the converter, when properly optimized as discussed in chapter 3. Any method to recycle some of the gate charge can go a long way towards improving the efficiency of the converter. However, as the gates of the power devices must be well-controlled to ensure a positive dead-time, some charge recycling methods cannot be used. For example, the capacitor shorting method in section 8.3.2 cannot be used as it directly charges one capacitance from the other. If that method is used for gate charge recovery, both phase 1 and phase 2 switches would be on simultaneously, potentially allowing excessive short-circuit currents to flow in the converter.

In macro-scale two-phase SC converters, using a multiple-winding transformer to perform the gate drive allows for both source isolation and gate resonance [4]. The power transistor gates are directly driven at the resonance between the magnetizing inductance of the transformer and the total gate capacitance. The primary winding is driven from a bias supply through a resonance-sensing circuit using fixed-width excitation pulses. Each gate is driven with its own secondary winding, with polarity connected according to switch phase. Since SC converters are not particularly sensitive to duty cycle, a pure zero-centered sine wave is applied to each gate. This ensures sufficient dead-time and a simple control scheme. In [4], the resonant gate drive reduces overall converter loss by 33 percent in a discrete-component implementation.

In an integrated converter, creating this transformer is nearly impossible. Integrated inductors, in addition to the metal needed to distribute the gating signal, are too resistive to exhibit sufficiently-high quality factors to make an integrated resonant gate drive scheme practical. Additionally, the requirement of non-overlapping gate drive signals make SC-

based charge sharing schemes difficult to implement. Such a scheme would require a long switch dead-time to enable several periods of charge transfer switching. For medium- to high-frequency integrated SC converters, gate energy recycling is not yet feasible.

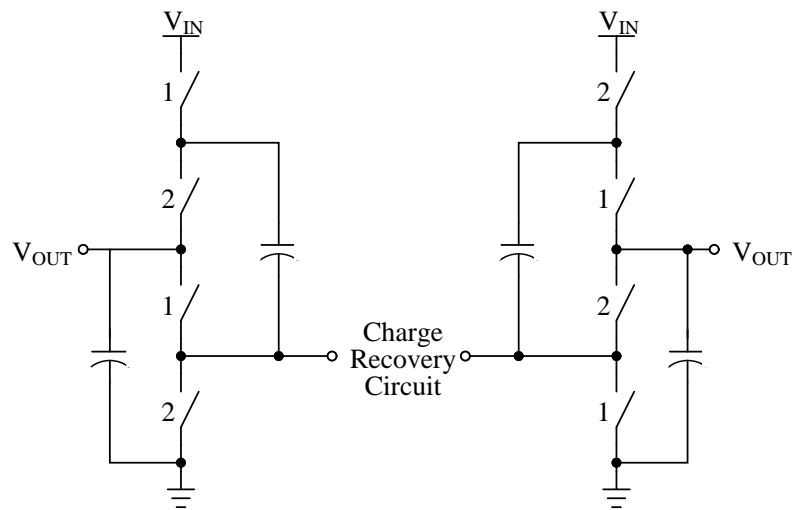
8.3.2 Drain Charge Recovery

The drain-source parasitic capacitance of the power transistors also consumes a significant fraction of the power loss in an SC converter. However, as the voltage across this parasitic capacitance does not control the switch state, it can be manipulated more flexibly than the gate capacitance. If we assume the output and input sources are low-impedance, and the flying capacitors are much larger than the total circuit parasitic capacitors, we note that all the drain parasitic capacitances connect the flying node associated with a flying capacitor and incremental ground. Thus, all of these parasitics, in addition to the bottom-plate parasitic capacitance of the flying capacitors, are in parallel. Using a single charge-recovery circuit per flying capacitor, the effects of nearly all the drain and bottom plate capacitances will be reduced.

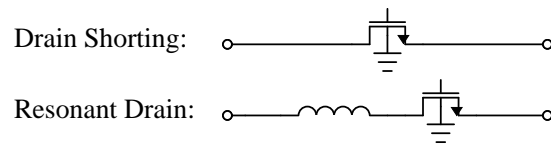
Using a simple 2:1 circuit as an example, such as one of the two interleaved phases shown in figure 8.7a, drain charge recovery will be demonstrated. With a single 2:1 circuit, the parasitic capacitance is charged during phase 1 and discharged during phase 2. If two such circuits are interleaved, i.e. clocked 180 degrees apart, the charge recovery circuit can transfer charge between the parasitic capacitances of each phase during the dead-time between switching periods. In a 2:1 converter, since each interleaved phase only has a single flying capacitor, the charge recovery circuitry can connect to the bottom terminal of the flying capacitor², as shown in figure 8.7a.

Two charge recovery methods will be discussed here, both shown in figure 8.7b. The first method, designated *drain shorting*, uses a single power transistor that is turned on during the dead-time between each primary phase (thus, twice per period). This conductance path equalizes the voltage on each of the two equivalent parasitic drain capacitances. Thus,

²Alternately, the charge recovery circuit can be connected to each of the top nodes of the flying capacitors



(a) 2:1 ladder interleaved phases, noting terminals used for charge recovery



(b) charge recovery circuits

Figure 8.7. Drain charge recovery using a two-interleaved-phase 2:1 converter

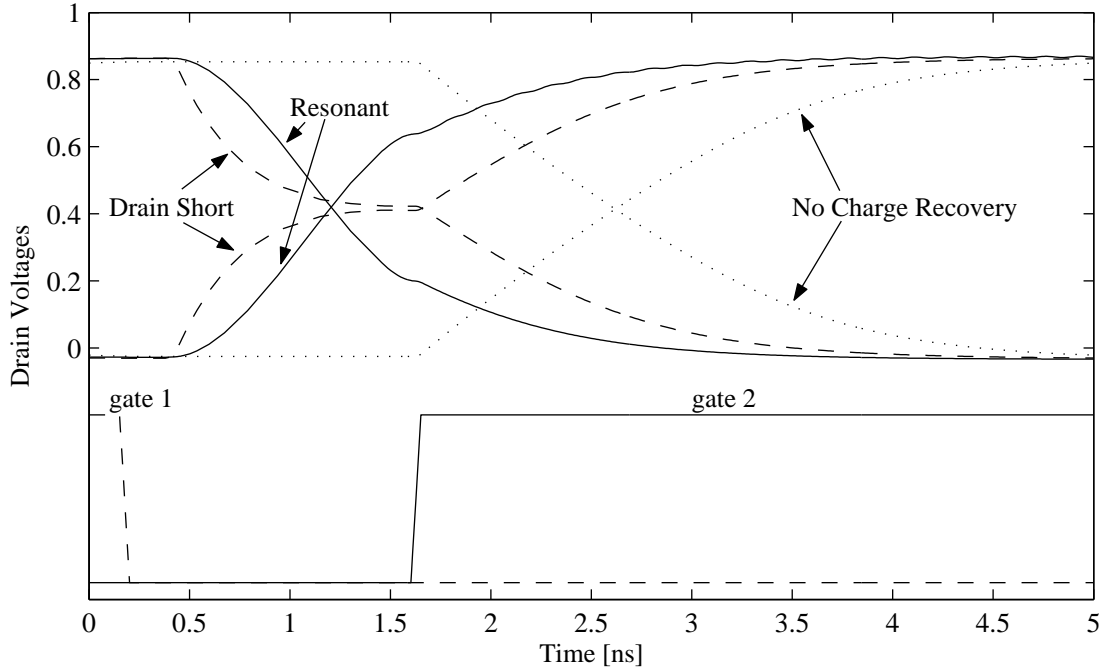


Figure 8.8. Waveforms of drain charge recovery methods

during the next phase, the amount of charge needed to charge the parasitic capacitance is reduced approximately by a factor of two.

The second method, denoted *resonant drain*, uses an inductor to transfer the charge from the parasitic capacitance in one interleaved phase to the opposite capacitance. If the current path was lossless, this transfer of charge would be complete, eliminating the drain parasitic and bottom-plate parasitic loss. However, as the path resistance is finite, there will be some loss using this method. In entirely-integrated converters, the area cost due to this inductor must be considered. Additionally, careful layout must be performed to ensure this R-L charge transfer network has a quality factor greater than one. If the resonant drain method is not feasible, the drain shorting method can be used.

Figure 8.8 shows a single phase transition of the converter shown in figure 8.7a. The size of the shorting transistor is similar to each of the power transistors in the circuit. An inductance of 30 nH is used to transfer the charge between the 10 pF parasitic drain capacitances. The voltage at the negative terminal of both of the flying capacitors is shown

for each of the two recovery methods and without any charge recovery method. Both methods cause the drain voltages to partially transition to the opposite state during the dead-time of the primary phase clocks. The drain shorting method recovers approximately half of the drain charge, while this implementation of the resonant charge method recovers about 75% of the parasitic charge. In both cases, the dead-time must be sufficiently large to enable a charge-recovery pulse between main phase clocks.

Using either of these charge recovery methods, or any other parasitic reduction method, modifies portions of the power loss equation. Thus, when a parasitic reduction method is used, the converter must be re-optimized while accounting for the modifications to yield a new optimal design.

8.3.3 Reducing Bottom-Plate Capacitance

The previous two sections (8.3.1 and 8.3.2) discuss additional circuits that reduce the power lost to two different parasitic capacitances in an SC converter. This section discusses improvements to the layout of MOS-based capacitors to reduce their bottom-plate parasitic capacitance. This improvement originates from two adjustments. First, the area of each capacitor cell is maximized. Second, the n-well for a PMOS-based capacitor should be biased appropriately.

MOS capacitors for SC converters are typically made using PMOS-based capacitors³ or triple-well NMOS capacitors. This section will examine PMOS-based capacitors as they require no special processing steps. Thus, the n-well diffusion capacitance of the capacitor cell is the dominant parasitic of the capacitor. Since the capacitance of a junction is related to both the area and perimeter of the well, but the primary oxide capacitance is only related to area, the ratio of parasitic to primary capacitance can be minimized by making the cell (and thus its n-well) as large and as square as the design rules for the process allow.

Next, the terminals must be biased correctly in order to minimize the parasitic capacitance. For maximum primary capacitance, the source and drain of the PMOS-based device

³Assuming a p-doped substrate

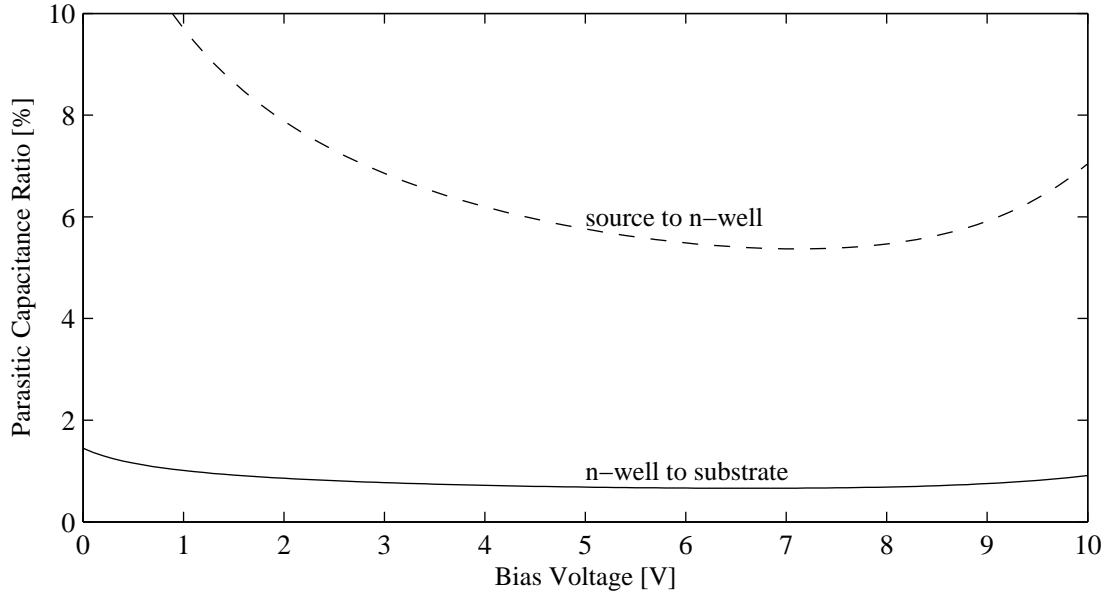


Figure 8.9. Parasitic capacitance ratios for body and well capacitances

are connected together and used as the positive terminal. The gate of the device is used as the negative terminal. However, flexibility exists in the biasing of the capacitor's n-well. Two junction capacitances are connected to the n-well tie: the source-well capacitance and the well-substrate capacitance. Based on how the n-well is biased, either of these capacitances can act as the bottom-plate capacitance of the device. Finally, if a DC voltage is used to bias the n-well against either the substrate or source, the diffusion capacitance can be made smaller. In this analysis, the source to substrate voltage remains low while the n-well bias voltage is adjusted.

Figure 8.9 shows a graph of the ratio between the parasitic bottom-plate capacitance and the primary capacitance. A PMOS-based capacitor made with $2\ \mu\text{m}$ long transistor fingers and well dimensions of $40\ \mu\text{m}$ by $40\ \mu\text{m}$ was simulated in a 65 nm process. One curve shows the bottom-plate parasitic if the well is tied to a DC potential above the substrate, such that the source-well capacitance becomes the bottom-plate capacitance. The second curve shows the same ratio if the well was tied to a DC potential above the source, shorting the source-well capacitance, such that the well-substrate junction capacitance becomes the bottom-plate capacitance. When the n-well is biased above the source of the transistor by

5 volts, the bottom-plate parasitic ratio becomes 0.7%, which is an impressively-low ratio for a MOS capacitor.

By using these methods of reducing the bottom-plate parasitic capacitance, higher power densities can be obtained for the same efficiency. These parasitic-reduction methods provide the necessary efficiency improvements to make microprocessor-level SC converters practical.

Chapter 9

Conclusions

This work has developed both fundamental analysis and practical design methods for switched-capacitor (SC) DC-DC power converters. SC converters can be used for numerous applications in the power conversion space, since they have numerous advantages over traditional inductor-based power converters. First, since they use no inductors, SC converters can be easily integrated on a silicon chip or into other applications where magnetics are impractical. In section 4.4, SC converters were shown to have superior silicon and reactive element utilization compared with traditional magnetics-based converters such as the buck and boost converters. In chapter 7, SC converters were shown to operate efficiently over many orders of magnitude of power, which is difficult for many inductor-based converters. Although inductor-based converters perform regulation highly efficiently, regulation is possible using SC converters as discussed in chapter 5. These advantages strongly motivate the use of SC converters in many applications.

In the analysis chapters of this work, chapters 2 through 4, a thorough but simple analysis method was developed that predicts the output resistance and efficiency of an SC converter. The foundation of this method relies on *charge multipliers*, the ratio of the charge flowing through a component to the output charge flow. The charge multipliers for any SC topology can be found by simple inspection or using the circuit-theoretic method discussed in appendix A. These charge multipliers allow for the simple calculation of output

impedance, which, in turn, allows the optimal sizing of both the capacitors and switches in an SC converter. System-wide switch area and switching frequency were optimized to yield the minimal power loss at a specific design point in chapter 3. A MATLAB-based tool can automate these design methodologies to enable rapid evaluation of SC topologies as discussed in appendix B. These design methodologies enable the optimal design of SC converters for any application, from sensor nodes to microprocessors and more.

Three applications for SC converters were discussed in chapters 6 through 8. By using a hybrid boost-SC converter topology, a high voltage was generated with maximal efficiency with a converter of minimum mass. This converter was used to control piezoelectric actuators on a two-gram MicroGlider, as reported in chapter 6. Since many SC topologies can be run in an open-loop configuration, the drive strategies for them are often simpler than for an inductor-based converter.

Chapter 7 described a power conversion and conditioning integrated circuit used for an energy-harvesting wireless sensor node. In this application, two on-die SC converters were used to generate system voltage rails of 2.1 and 0.7 volts from a 1.2 volt battery. SC converters were found to be superior to inductor-based converters in miniature sensor node systems as they can be fully integrated and they run efficiently down to microwatt levels.

Finally, SC converters can be used for significantly higher power densities and higher levels of integration than traditional magnetics-based converters. Chapter 8 describes a specific nine-switch topology for applications in powering microprocessors. In a 32-nm process, the area required to perform on-die power conversion is approximately 13%. As CMOS technology advances, the power density of SC converters increases, while the power produced by typical microprocessors remains approximately constant due to thermal constraints. Total processor die area also remains approximately constant as the number of transistors increases to counter process scaling. Thus, if on-die SC converters are used in the future, they will occupy an ever-decreasing percentage of the die. On-die SC converters are advantageous over external inductor-based converters since they can provide local supplies for each core in a many-core processor. Additionally, SC converters can have

extremely-fast transient responses compared with inductor-based converters where the inductor current limits response time. SC converters can better respond to the fast load transients associated with computational blocks turning on and off. SC converters may replace inductor-based converters in even high-power, high-performance applications due to these advantages.

Throughout this work, SC converters have been found to be simple to analyze, enabling the creation and analysis of many topologies. The design methods developed allow intelligent, optimized design of SC converters for many applications. Indeed, SC converters need not be limited to low-power, unregulated designs but can expand to compete with traditional converters in all realms of power conversion.

Appendix A

Network-Theory-Based Analysis for Switched-Capacitor Converters

The analysis methods presented in chapter 2 are sufficient when a converter's charge multipliers can be found by inspection. For more-complex topologies, or to automate the analysis of switched-capacitor (SC) converters, a network-theory based analysis method is needed. In addition, by developing the theory of SC converters, a greater understanding of the constraints behind the formulation and operation of SC converters can be obtained. This chapter is based on reference [27] and uses the theory presented in reference [13]. The section will first start by summarizing the relevant circuit theory, including the *fundamental loop matrix* and the *fundamental cut-set matrix*. Next, these methods are extended to SC converters and the capacitor charge multipliers are derived. A few theorems on properties of SC converters are stated and proven. The dynamics of SC converters will then be investigated from a network-theoretic standpoint.

A.1 Summary of Circuit Theory

Circuit theory is based on using specific techniques to mathematically describe electrical circuits. This section describes the procedure for extracting network parameters from

a circuit. For any electrical circuit, a directed graph (digraph) can be constructed which represents the topology of the circuit while discarding the properties of individual circuit elements. The reference direction of a circuit branch determines the direction of its representative branch in the digraph. The arrow on each branch represents the reference direction of that branch. Thus, the power dissipated by a given element, denoted by index i , is given by:

$$P_i = i_i v_i \quad (\text{A.1})$$

From a connected digraph \mathbf{G} , a tree \mathbf{T} can be constructed from selected branches of the digraph. While more than one tree can exist for any digraph, each tree \mathbf{T} must have the following properties:

1. \mathbf{T} is connected (i.e. there is a path through \mathbf{T} connecting any two nodes).
2. \mathbf{T} contains all the nodes in digraph \mathbf{G} .
3. \mathbf{T} contains no loops.

Figure A.1a shows a simple electric circuit which is then represented as a digraph in figure A.1b. Each component is transformed into a branch in the digraph where the direction of the arrow indicates the polarity of that component.

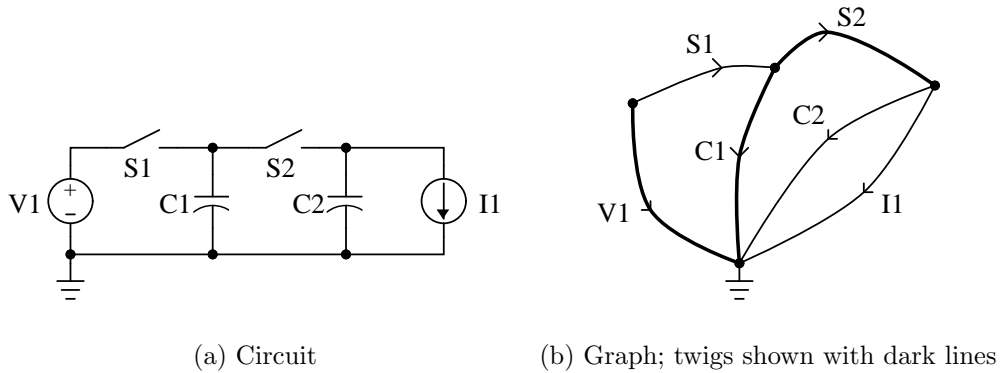


Figure A.1. An example circuit with graph representation

Each branch in digraph \mathbf{G} can be categorized as either a *twig* if it is contained in the tree \mathbf{T} or a *link* if it is not. For a digraph with n nodes and b branches, there are $n - 1$ twigs and $l = b - n + 1$ links. Twigs and links have the following important properties:

- For each link, there is a unique path along tree \mathbf{T} connecting the two endpoints of the link. This link and set of twigs in the path form the *fundamental loop* associated with the link.
- For each twig in \mathbf{T} , there exists a unique set of links such that a closed path can be drawn through the twig and the set of links such that the graph's nodes are split into two non-empty disjoint sets. This twig and set of links form the *fundamental cut set* associated with that twig.

These fundamental loops and fundamental cut sets depend on the selection of tree \mathbf{T} , but again are unique given a choice of tree.

Based on the choice of tree, the branch currents i_i and voltages v_i can be grouped into vectors \mathbf{i} and \mathbf{v} of dimension b with the links occurring first and the twigs last. Thus,

$$\mathbf{i} = \begin{bmatrix} i_1 \\ \vdots \\ i_l \\ i_{l+1} \\ \vdots \\ i_b \end{bmatrix} \quad \mathbf{v} = \begin{bmatrix} v_1 \\ \vdots \\ v_l \\ v_{l+1} \\ \vdots \\ v_b \end{bmatrix} \quad (\text{A.2})$$

Kirchoff's Voltage Law (KVL) states that the voltages around a closed loop sum to zero. Thus, the voltages around any fundamental loop can be summed and set equal to zero. Following the loop around in the direction given by the corresponding link's direction, each twigs' voltage is summed positively if its direction is the same as the link's direction, or subtracted if its direction opposes that of the link. For each link in \mathbf{G} , a KVL equation can be constructed from its fundamental loop. For a digraph with l links, l equations exist,

which can be formed into one matrix equation:

$$\mathbf{B}\mathbf{v} = 0. \quad (\text{A.3})$$

\mathbf{B} is the *fundamental loop matrix* of size $l \times b$ where each element is either 0, 1 or -1 . Since each fundamental loop contains only one link, \mathbf{B} can be written in the form:

$$\mathbf{B} = \begin{bmatrix} \mathbf{1}_l & \mathbf{B}_t \end{bmatrix} \quad (\text{A.4})$$

where $\mathbf{1}_l$ is an $l \times l$ identity matrix.

Similarly, Kirchoff's Current Law (KCL) states that the sum of currents going into a node (or subgraph) is equal to zero. For each fundamental cut set of the digraph \mathbf{G} , the currents through each element in the cut set in the direction of the selected subgraph must sum to zero. If the defining twig of a cut set points from subgraph A to subgraph B , the links in the cut set that also point from A to B are added positively. Links in the cut set that point the opposite direction are instead subtracted. For a network with $n - 1$ twigs, the $n - 1$ fundamental cut set equations can be formed into a matrix equation:

$$\mathbf{Q}\mathbf{i} = 0 \quad (\text{A.5})$$

where \mathbf{Q} is the *fundamental cut set matrix* corresponding to the digraph \mathbf{G} and the tree \mathbf{T} . The fundamental cut set matrix is the dual of the fundamental loop matrix and is related by the following relationship [13]:

$$\mathbf{Q} = \begin{bmatrix} \mathbf{Q}_l & \mathbf{1}_{n-1} \end{bmatrix} = \begin{bmatrix} -\mathbf{B}_t^\top & \mathbf{1}_{n-1} \end{bmatrix} \quad (\text{A.6})$$

A.2 Modeling Switched-Capacitor Networks

This section will derive the component voltages and charge multipliers for an SC converter based on fundamental network-theory-based methods. In this section, only properly-posed single-input, single-output two-phase converters will be considered, as specified in chapter 2. Further study of the proper formation of SC converters is presented in section A.3.

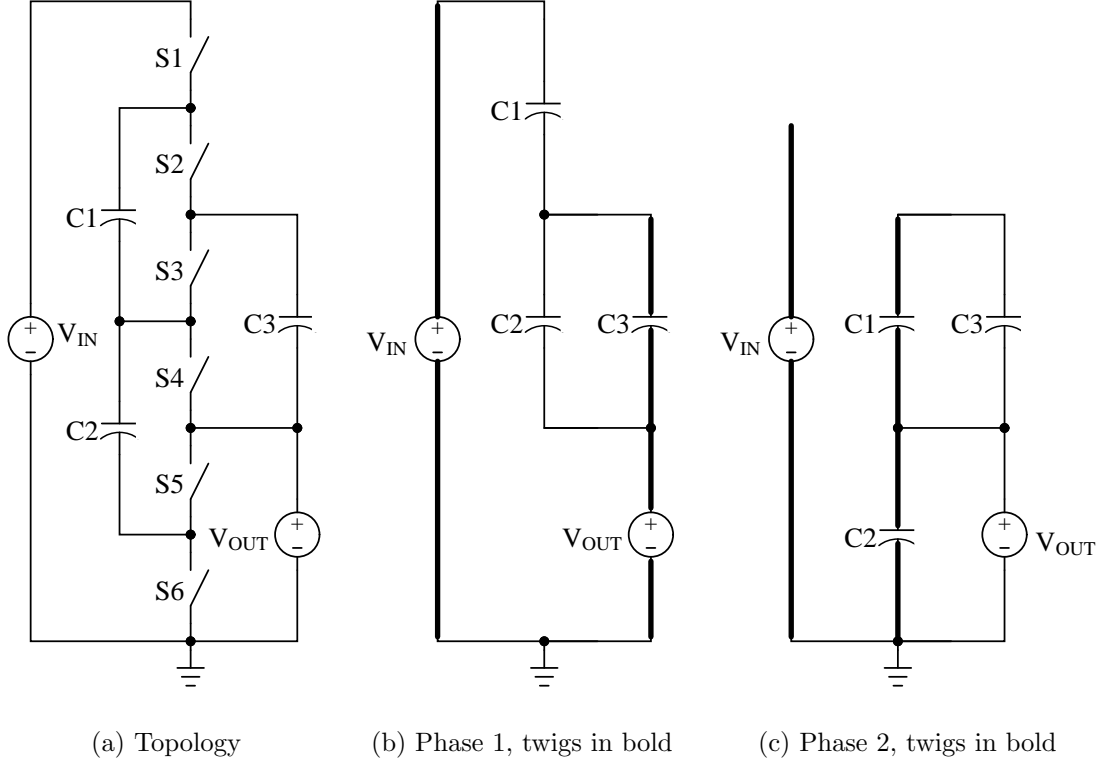


Figure A.2. 3:1 Ladder topology, including twig designations in each phase

In this section, a 3:1 ladder converter will be used as an example, as shown in figure A.2a. Figures A.2b and A.2c show the phase networks (i.e. capacitor configurations) in phases 1 and 2, respectively. For each phase network, a tree \mathbf{T}_1 or \mathbf{T}_2 can be constructed. The twigs in each tree are shown in bold (although the links and twigs depend on the choice of tree). This set of links and twigs will be used as an example in the following analysis. For a properly-posed two-phase converter, it is possible to choose the trees \mathbf{T}_1 and \mathbf{T}_2 such that each capacitor and output voltage source is a twig in one phase and a link in the other. In addition, the input source is classified as a twig in both phases. This section considers only properly-posed two-phase, two-port SC converters.

A.2.1 Finding the Conversion Ratio and Component Voltages

For each phase, a fundamental loop matrix can be constructed based on that phase's network. Unlike section A.1, the voltages will not be sorted link-first, as that sorting is not

consistent between phases. Instead, the voltage vector will be defined as:

$$\mathbf{v} = \begin{bmatrix} V_{IN} \\ v_{c1} \\ \vdots \\ v_{ck} \\ V_{OUT} \end{bmatrix}. \quad (\text{A.7})$$

From the two phase networks, two KVL equations based on the fundamental loop matrices are obtained as follows:

$$\mathbf{B}^1 \mathbf{v} = \mathbf{0} \quad \quad \quad \mathbf{B}^2 \mathbf{v} = \mathbf{0} \quad (\text{A.8})$$

To find the nominal conversion ratio and component voltages, the output current is assumed to be zero, so each capacitor must maintain a constant voltage in steady state. Thus, the phase-based KVL equations in (A.7) must hold simultaneously.

$$\mathbf{B} \mathbf{v} = \begin{bmatrix} \mathbf{B}^1 \\ \mathbf{B}^2 \end{bmatrix} \mathbf{v} = \mathbf{0} \quad (\text{A.9})$$

For example, the \mathbf{B} matrix and the corresponding KVL equation for the three-capacitor ladder converter would be:

$$\begin{bmatrix} -1 & 1 & 0 & 1 & 1 \\ 0 & 0 & 1 & -1 & 0 \\ 0 & -1 & 0 & 1 & 0 \\ 0 & 0 & -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{IN} \\ v_{c1} \\ v_{c2} \\ v_{c3} \\ V_{OUT} \end{bmatrix} = \mathbf{0} \quad (\text{A.10})$$

By inspection, the matrix in (A.10) has rank 4. Thus, this KVL equation has a single degree of freedom, which corresponds to the input voltage. All voltages in the unloaded circuit can be found in terms of the input voltage by manipulating (A.10).

In order to find the converter voltages in terms of the input voltage, the \mathbf{B} matrix will

be partitioned as follows:

$$\left[\begin{array}{c|cccc} -1 & 1 & 0 & 1 & 1 \\ 0 & 0 & 1 & -1 & 0 \\ 0 & -1 & 0 & 1 & 0 \\ 0 & 0 & -1 & 0 & 1 \end{array} \right] \begin{bmatrix} V_{IN} \\ v_{c1} \\ v_{c2} \\ v_{c3} \\ V_{OUT} \end{bmatrix} = \begin{bmatrix} \mathbf{b}_{in} & \mathbf{B}_c \end{bmatrix} \begin{bmatrix} V_{IN} \\ \mathbf{v}_c \\ V_{OUT} \end{bmatrix} = 0 \quad (\text{A.11})$$

From (A.11), the capacitor and output voltage vector can be found simply by solving (A.12), since \mathbf{B}_c is square and full-rank for properly-posed converters:

$$\mathbf{B}_c \begin{bmatrix} \mathbf{v}_c \\ V_{out} \end{bmatrix} = -\mathbf{b}_{in} V_{IN}. \quad (\text{A.12})$$

This method can be used to find the capacitor voltages and output voltage for the 3:1 ladder converter in terms of the input voltage:

$$\begin{bmatrix} v_{c1} \\ v_{c2} \\ v_{c3} \\ V_{out} \end{bmatrix} = - \begin{bmatrix} 1 & 0 & 1 & 1 \\ 0 & 1 & -1 & 0 \\ -1 & 0 & 1 & 0 \\ 0 & -1 & 0 & 1 \end{bmatrix}^{-1} \begin{bmatrix} -1 \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{IN} = \begin{bmatrix} 1/3 \\ 1/3 \\ 1/3 \\ 1/3 \end{bmatrix} V_{IN}. \quad (\text{A.13})$$

Thus, each of the capacitors in the circuit supports one-third of the input voltage, and the converter has a conversion ratio of 1/3. While these numbers can easily be determined by inspection, for more complicated converters or for use in an automated design tool, this method can be used to determine conversion ratio and component voltages.

A.2.2 Determining the Charge Multiplier Vector

So far, unloaded SC networks have been considered where capacitor voltages are constant and no current flows in the converter. When the load current is non-zero, the capacitor voltages change during phase transitions, but reach a periodic-steady-state pattern under constant line and load operating conditions. The charge multipliers, the ratio of charge flow

in a component to the output charge flow, is derived here, based on a network theoretic formulation. As in section 2.1, this analysis will assume operation in slow-switching limit (SSL) and will thus neglect the small on-state resistance of the switches in the converter.

To transfer charge between input and output, charge must be transferred between the capacitors. In steady state, the capacitor voltages are in periodic steady state. Because operation in the SSL is being considered, there is an impulsive charge transfer, represented by $\Delta \mathbf{q}_2$ during the transition from phase 1 to phase 2, and another charge transfer $\Delta \mathbf{q}_1$ during the opposite transition. Over an entire clock period, no net current flows in each capacitor, and thus $\Delta \mathbf{q}_1$ and $\Delta \mathbf{q}_2$ obey the following relationship:

$$\Delta \mathbf{q}_c^1 = -\Delta \mathbf{q}_c^2 \quad (\text{A.14})$$

where $\Delta \mathbf{q}_c^1$ and $\Delta \mathbf{q}_c^2$ are the components of $\Delta \mathbf{q}^1$ and $\Delta \mathbf{q}^2$, respectively, that correspond to the capacitors. Since $\Delta \mathbf{q}$ is an integrated current (charge flow), it must satisfy KCL for each phase transition:

$$\mathbf{Q}^j \Delta \mathbf{q}^j = \mathbf{0} \quad (\text{A.15})$$

where \mathbf{Q}^j is the fundamental cut-set matrix for the transition in phase j , and can be found by using the methods in section A.1 or from the identity in equation A.6.

By examining the fundamental cut-sets for the phase 1 and 2 networks in figures A.2b and A.2c, respectively, the KCL equations for the ladder converter can be found:

$$\begin{bmatrix} 0 & -1 & 0 & 0 & 1 \\ 0 & -1 & 1 & 1 & 0 \\ 1 & 1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \Delta Q_{IN}^1 \\ \Delta q_{c1}^1 \\ \Delta q_{c2}^1 \\ \Delta q_{c3}^1 \\ \Delta Q_{OUT}^1 \end{bmatrix} = 0 \quad \begin{bmatrix} 0 & 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \Delta Q_{IN}^2 \\ \Delta q_{c1}^2 \\ \Delta q_{c2}^2 \\ \Delta q_{c3}^2 \\ \Delta Q_{OUT}^2 \end{bmatrix} = 0 \quad (\text{A.16})$$

Using the identity in equation A.14, the two KCL equations in (A.16) can be combined to form a system of equations including both ΔQ_{OUT}^1 and ΔQ_{OUT}^2 . Since the charge multipliers represent the charge flows in terms of the output current, the following transformation will

be used to convert ΔQ_{OUT} and $\Delta Q_{OUT,diff} = \Delta Q_{OUT,2} - \Delta Q_{OUT,1}$:

$$\begin{bmatrix} \Delta Q_{OUT,diff} \\ \Delta Q_{OUT} \end{bmatrix} = \mathbf{T}_Q \Delta \mathbf{q} = \begin{bmatrix} -1 & 1 \\ 1 & 1 \end{bmatrix} \begin{bmatrix} \Delta Q_{OUT}^1 \\ \Delta Q_{OUT}^2 \end{bmatrix} \quad (\text{A.17})$$

This transformation can then be applied to (A.16) to create a single KCL matrix equation:

$$\mathbf{Q} \Delta \mathbf{q} = \begin{bmatrix} \mathbf{Q}_1 \\ \mathbf{Q}_2 \end{bmatrix} \begin{bmatrix} \mathbf{I} \\ \mathbf{T}_Q^{-1} \end{bmatrix} \Delta \mathbf{q} = 0 \quad (\text{A.18})$$

Substituting (A.16) into (A.18) in the case of the ladder converter yields:

$$\begin{bmatrix} 0 & 0 & -1 & 0 & 0 & -1/2 & 1/2 \\ 0 & 0 & -1 & 1 & 1 & 0 & 0 \\ 1 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 1/2 & 1/2 \\ 0 & 0 & -1 & 0 & -1 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \Delta Q_{IN}^1 \\ \Delta Q_{IN}^2 \\ \Delta q_{c1}^1 \\ \Delta q_{c2}^1 \\ \Delta q_{c3}^1 \\ \Delta Q_{OUT,diff} \\ \Delta Q_{OUT} \end{bmatrix} = 0 \quad (\text{A.19})$$

The transformed two-phase fundamental cut-set matrix \mathbf{Q} for the ladder converter has a rank of 6. The single degree of freedom in this equation corresponds to the output current ΔQ_{OUT} . To solve the charge flows in terms of the output current, \mathbf{Q} will be partitioned as follows:

$$\mathbf{Q} \Delta \mathbf{q} = \begin{bmatrix} \mathbf{Q}_C & \mathbf{q}_{out} \end{bmatrix} \begin{bmatrix} \Delta Q_{IN}^1 \\ \Delta Q_{IN}^2 \\ \Delta \mathbf{q}_c \\ \Delta Q_{OUT,diff} \\ \Delta Q_{OUT} \end{bmatrix}. \quad (\text{A.20})$$

Since \mathbf{Q}_C is square and full-rank for properly-posed converters, as discussed in section

A.3, the currents are fully specified by the topology, and can be found by:

$$\mathbf{Q}_C \begin{bmatrix} \Delta Q_{IN}^1 \\ \Delta Q_{IN}^2 \\ \Delta q_c \\ \Delta Q_{OUT,diff} \end{bmatrix} = -\mathbf{q}_{out} \Delta Q_{OUT}. \quad (\text{A.21})$$

Using the ladder converter example KCL equations in (A.19), the current flow in the converter can be found as:

$$\begin{bmatrix} 0 & 0 & 0 & -1 & 0 & 1/2 \\ 0 & 0 & -1 & 0 & -1 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & -1/2 \\ 0 & 0 & -1 & 1 & 1 & 0 \\ 1 & 0 & 1 & 0 & 0 & 0 \end{bmatrix}^{-1} \begin{bmatrix} \Delta Q_{IN}^1 \\ \Delta Q_{IN}^2 \\ \Delta q_{c1} \\ \Delta q_{c2} \\ \Delta q_{c3} \\ \Delta Q_{OUT,diff} \end{bmatrix} = - \begin{bmatrix} 1/2 \\ 0 \\ 0 \\ 1/2 \\ 0 \\ 0 \end{bmatrix} \Delta Q_{OUT} \quad (\text{A.22})$$

$$\begin{bmatrix} \Delta Q_{IN}^1 \\ \Delta Q_{IN}^2 \\ \Delta q_{c1} \\ \Delta q_{c2} \\ \Delta q_{c3} \\ \Delta Q_{OUT}^2 - \Delta Q_{OUT}^1 \end{bmatrix} = \begin{bmatrix} -1/3 \\ 0 \\ 1/3 \\ 2/3 \\ -1/3 \\ 1/3 \end{bmatrix} \Delta Q_{OUT}. \quad (\text{A.23})$$

Equation (A.22) determines the charge flows in the converter in terms of the output current. Thus, the charge multipliers for the capacitors can easily be determined by extracting the terms in (A.23) corresponding to the capacitors:

$$\begin{bmatrix} a_{c1} \\ a_{c2} \\ a_{c,3} \end{bmatrix} = \begin{bmatrix} 1/3 \\ 2/3 \\ -1/3 \end{bmatrix}. \quad (\text{A.24})$$

The methods in this chapter develop a straightforward circuit theory based method for determining component voltages and charge multipliers for any SC converter. This

method can be used for complex topologies where determining the values by inspection is inconvenient. Additionally, if a computer-based SC analysis program is needed, this method can be used.

Switch Charge Multiplier Vectors

To determine the SSL charge multipliers, the resistance drops across the converter's switches were neglected. However, in the FSL, the switch on-state resistance is the dominant converter loss. Since the currents in the circuit are still constrained by the topology, as in section A.2.2, the capacitor charge flows are the same as calculated above.

When the open and closed switches are added to the phase networks of a converter, they can be incorporated in both the KVL and KCL equations to determine their charge flows and blocking voltages. In each of the phase networks, the closed switches are *usually* twigs, as they connect two nodes which ordinarily would be the same node in a capacitor-only tree.¹ The current through an on-state switch can be related to the capacitor currents by finding the fundamental cut-set corresponding to that switch during the phase which it is on. The resulting equation relates the currents in this switch to the currents through the link capacitors. Two matrix equations can be constructed representing the currents through the on-state switches in each phase:

$$i_r^1 = Q_{RC}^1 i_c^1 \qquad i_r^2 = Q_{RC}^2 i_c^2 \qquad (\text{A.25})$$

The Q_{RC}^1 and Q_{RC}^2 matrices are defined to include rows of zeros corresponding to the off-state switches to ease the dynamics calculation in section A.4. The two phase-based switch fundamental cut-set matrix relations for the 3:1 ladder converter, in figure A.2, are

¹Some switches in some topologies may be redundant from a graph theory perspective and are thus designated links.

as follows:

$$\mathbf{i}_r^1 = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ -1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{c1}^1 \\ i_{c2}^1 \\ i_{c3}^1 \\ i_{OUT}^1 \end{bmatrix}, \quad \mathbf{i}_r^2 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{c1}^2 \\ i_{c2}^2 \\ i_{c3}^2 \\ i_{OUT}^2 \end{bmatrix} \quad (\text{A.26})$$

To find the corresponding charge multiplier for each switch, the switch fundamental cut-set matrix where the corresponding row is non-zero is multiplied with the capacitor charge multipliers, and the output charge during that phase substituted for I_{OUT} :

$$\mathbf{a}_r^j = \mathbf{Q}_{RC}^j \begin{bmatrix} a_{c1}^j \\ a_{c2}^j \\ a_{c3}^j \\ i_{OUT}^j / I_{OUT} \end{bmatrix}, \quad \mathbf{a}_r = \mathbf{a}_r^1 + \mathbf{a}_r^2. \quad (\text{A.27})$$

Since the open switches connect two nodes that are already included in the tree, open-state switches are *always* links. The voltages across these open-state switches can be calculated in terms of the capacitor and input and output source voltages in the circuit, neglecting the voltage across the on-state switches. Fundamental loop equations can be created involving each off-state switch and the twig capacitors and sources.² The switch blocking voltages can be found through the following KVL-like equations involving two phase-based switch fundamental loop matrices:

$$\mathbf{v}_r^1 = \mathbf{B}_{RC}^1 \mathbf{v}_c \quad \mathbf{v}_r^2 = \mathbf{B}_{RC}^2 \mathbf{v}_c \quad (\text{A.28})$$

The two phase-based switch fundamental loop matrix relations for the 3:1 ladder converter,

²If switch drops were included, the switch blocking voltage may vary slightly, depending on load.

in figure A.2, are as follows:

$$\mathbf{v}_r^1 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & -1 & -1 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{IN} \\ v_{c1} \\ v_{c2} \\ v_{c3} \\ V_{OUT} \end{bmatrix}, \quad \mathbf{v}_r^2 = \begin{bmatrix} 1 & -1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{IN} \\ v_{c1} \\ v_{c2} \\ v_{c3} \\ V_{OUT} \end{bmatrix} \quad (\text{A.29})$$

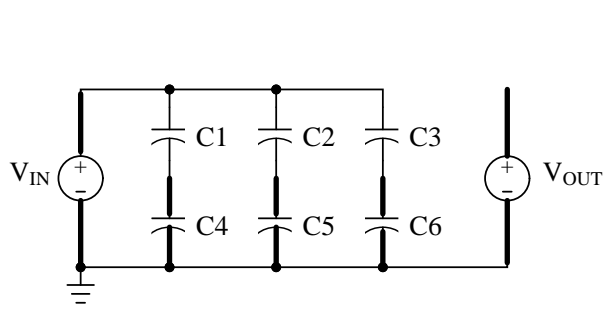
Since the voltages on the sources and capacitors are nearly constant in typical operation, the DC values of voltage, calculated in section A.2.1, are used in (A.29).

These matrices are used to find the currents through and voltages across the switches in the converter. They are also used to calculate converter dynamics in section A.4.

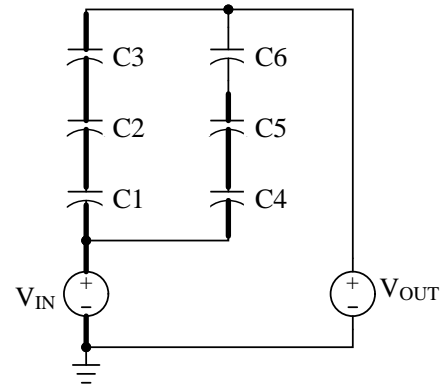
A.3 Criteria for Properly-Posed SC Topologies

While the assumption that properly-posed converters has been used throughout this work, little examination has been made on what properties a properly-posed converter has. First, the converters have been formulated to have a single input and output voltage source while eliminating unnecessary bypass (DC) capacitors. The following analysis will examine the fundamental loop matrix \mathbf{B}_C , in (A.11) and the fundamental cut-set matrix \mathbf{Q}_C , in (A.20). In the example in the previous section, the 3:1 ladder converter, these two matrices have been square and invertible. This criterium ensures that a converter is properly-posed. This section examines converters that are not properly-posed and modifications that can be used to make a converter properly-posed.

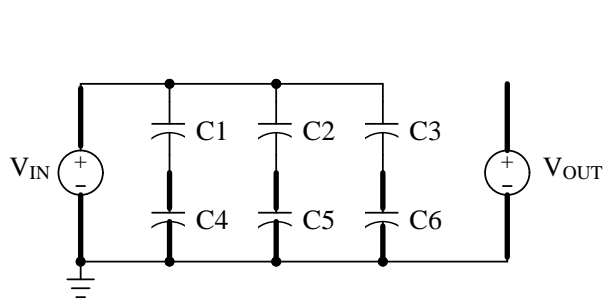
The next example will consider the 2:5 series-parallel topology, shown in figure 4.3. As shown, the two phase networks are shown in figures A.3a-b. The twig assignments for each network are shown in bold. By inspection, and the analysis in section 4.2.4, all formulations in figure A.3 perform the desired power conversion, however, only one is *properly-posed* (or



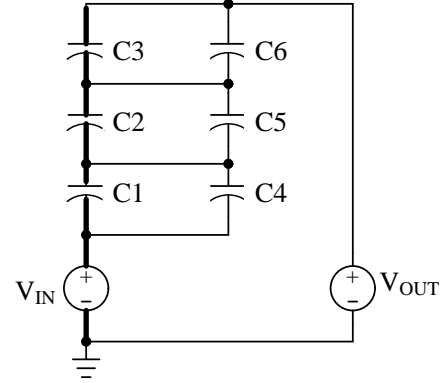
(a) Phase 1, original



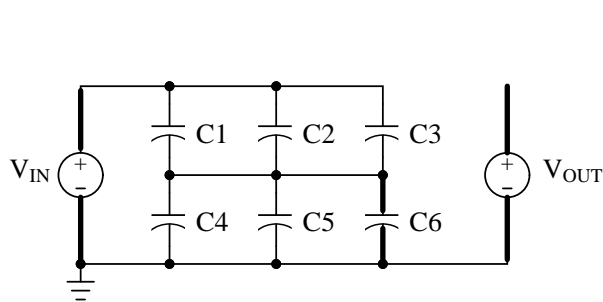
(b) Phase 2, original



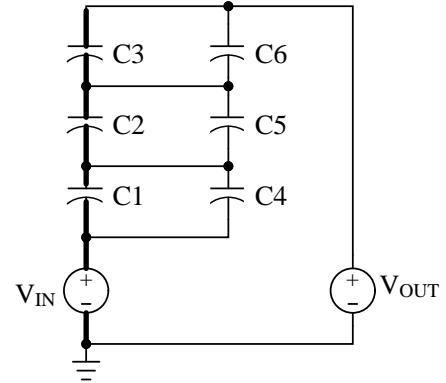
(c) Phase 1, 1 set equalizing switches



(d) Phase 2, 1 set equalizing switches



(e) Phase 1, 2 sets equalizing switches



(f) Phase 2, 2 sets equalizing switches

Figure A.3. Three configurations of a 2:5 series-parallel topology

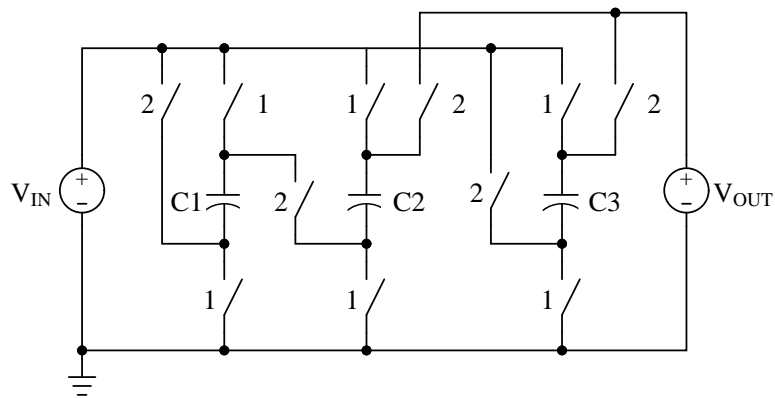
well-posed). In the first case, there are an excessive number of twigs in the two phase networks. With excessive twigs, the KVL equation is under-constrained (as there are few links to contribute equations). Since KVL cannot be solved, the DC voltages on each capacitor cannot be explicitly solved, but only a few relationships between the voltages can be found. Additionally, the fundamental cut-set matrix is no longer square, so the KCL equations may be over-constrained. While the converter can operate effectively, there is no guarantee on the capacitor voltages remaining below their limits, and therefore the converter is not properly-posed.

Figures A.3c-d show the networks if additional switches are connected in phase 2, as shown. These equalize the voltages between the capacitors in phase 2. In this configuration, both the fundamental loop matrix and fundamental cut-set matrix are square and full-rank. Thus, this converter is inherently properly-posed. Another indication that this converter is properly-posed is that each capacitor (and the output source) can be made a twig in one phase and a link in the other.

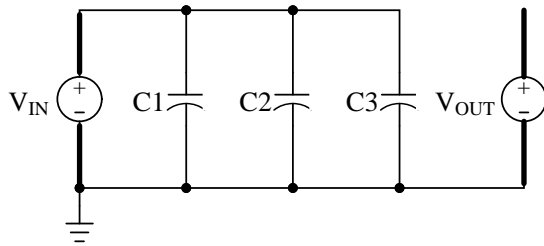
Figures A.3e-f show the phase networks if equalizing switches are added for both phase 1 and phase 2. In this case, the two networks have excessive links. As the dual of the first problem, capacitor currents are not constrained by the topology since the KCL equations are under-constrained. Instead, the capacitor currents are set in terms of the capacitor values with a few constraints from the KCL equations. The fundamental loop matrix is no longer square, resulting in over-constrained KVL equations. Since the KCL equation is under-constrained and the KVL equation is over-constrained, this converter is not properly-posed.

Next, a converter will be presented that is not properly-posed. Figure A.4 shows a converter which is a 1:3 series-parallel converter in parallel with a 1:2 series-parallel converter. The conversion ratio of this converter is undefined, as currents flow in the converter while unloaded. While it is clear by inspection that there is no steady-state zero-current solution to this converter, a look at the criteria defined in this section is useful.

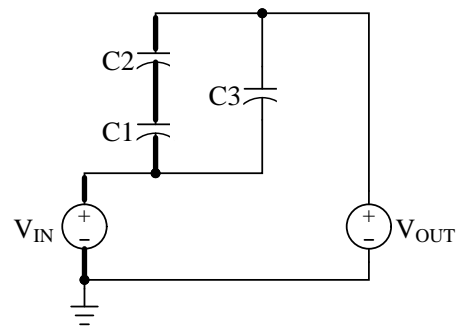
First, as C3 is never a twig in either of the two phase trees, it is evident that there are too



(a) Topology



(b) Phase 1 capacitor configuration



(c) Phase 2 capacitor configuration

Figure A.4. An improperly-posed switched-capacitor converter

many links in the phase trees. This suggests the KVL equations may be over-constrained. First, the fundamental loop equations will be written for both phases, and the equivalent of (A.10) will be formed:

$$\begin{bmatrix} -1 & 1 & 0 & 0 & 0 \\ -1 & 0 & 1 & 0 & 0 \\ -1 & 0 & 0 & 1 & 0 \\ 0 & -1 & -1 & 1 & 0 \\ -1 & -1 & -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{IN} \\ v_{c1} \\ v_{c2} \\ v_{c3} \\ V_{OUT} \end{bmatrix} = 0 \quad (\text{A.30})$$

where the first three rows correspond to phase 1, setting all the capacitor voltages equal to the input voltage. The last two rows correspond to phase 2. By inspection, since row 4 equates the voltage on capacitor C3 to the sum of the voltage on C1 and C2, no general solution exists. In fact, as this matrix \mathbf{B} has rank 5, it is invertible, and thus no degrees of freedom in the solution exists. The only solution to (A.30) corresponds to all voltages equalling zero. These observations independently show that this converter is not properly-posed.

Using the methods in this section, a systematic method of determining whether an SC converter is properly-posed, and thus suitable for analysis, has been developed.

A.4 Converter Dynamics

This section develops an exact model of the dynamics of an SC converter using the circuit-theory based analysis method developed in section A.2. In each clock period, the converter forms an R-C network based on the circuit's capacitors and on-state switches, modeled as resistances. The voltage on each capacitor approaches a steady-state value during each phase. In the next phase, another R-C network is formed with its own dynamics. Thus, an SC converter can be modeled as a continuous-time, time-dependent linear system, as can other switched-mode converters. If the system is integrated through a switching period, an alternate discrete-time linear system can be constructed where the sample time

corresponds to the period of the converter. The continuous-time and discrete-time linear systems will be found in terms of the fundamental network theory parameters found in section A.2.

A.4.1 Preparing the System

In this section, the complete dynamics of a converter will be considered. In particular, the ideal voltage source at the output port will be replaced with a current source in parallel with a capacitor. This replacement more-accurately describes most converter implementations and allows for the simulation of output voltage dynamics. In a properly-posed converter, this capacitor will be a link in one phase and a twig in another, like the original voltage-source load. The current source load is a link in both phases. The current through the output capacitor $\Delta Q_{COUT,2}$ is equal to half the ripple current at the output, denoted $\Delta Q_{OUT,2} - \Delta Q_{OUT,1}$ in (A.17). The output capacitor voltage is added to the voltage vector, replacing the output voltage component. The state voltage vector \mathbf{v} will be defined as follows:

$$\mathbf{v}_C = \begin{bmatrix} v_{c1} \\ v_{c2} \\ v_{c3} \\ v_{cout} \end{bmatrix} \quad (\text{A.31})$$

where the output voltage of the converter is equal to the fourth element of this vector.

Since the fundamental loop matrix \mathbf{B} is used in determining system dynamics in each phase, its separate phase components \mathbf{B}^1 and \mathbf{B}^2 from (A.9) will be used. For consistency, the rows of \mathbf{B}^j must be ordered according to the link used for each fundamental loop. For example, in phase 1 of the 3:1 ladder converter, the fundamental loop of C1 should be the first row of \mathbf{B}^1 , followed by the fundamental loop of C2. Each of the fundamental loop matrices \mathbf{B}^j can be subdivided into two components. The first matrix \mathbf{B}_C^j corresponds to the capacitor elements and vector \mathbf{b}_{IN}^j corresponds to the input source. The properly-ordered

and segmented fundamental loop matrices for the 3:1 converter are as follows:

$$\mathbf{B}^1 = \left[\begin{array}{c|cccc} -1 & 1 & 0 & 1 & 1 \\ 0 & 0 & 1 & -1 & 0 \end{array} \right], \quad \mathbf{B}^2 = \left[\begin{array}{c|cccc} 0 & -1 & 0 & 1 & 0 \\ 0 & 0 & -1 & 0 & 1 \end{array} \right]. \quad (\text{A.32})$$

The switch fundamental cut-set matrices \mathbf{Q}_{RC}^j will be simplified by eliminating the columns of zeros which correspond to twig capacitors. These reduced switch cut-set matrices will be denoted \mathbf{Q}_{RCx}^j to distinguish them from the full matrices. The reduced switch cut-set matrices for the 3:1 ladder converter example are given as follows:

$$\mathbf{Q}_{RCx}^1 = \left[\begin{array}{cc} 1 & 0 \\ 0 & 0 \\ -1 & 1 \\ 0 & 0 \\ 0 & -1 \\ 0 & 0 \end{array} \right], \quad \mathbf{Q}_{RCx}^2 = \left[\begin{array}{cc} 0 & 0 \\ -1 & 0 \\ 0 & 0 \\ 1 & -1 \\ 0 & 0 \\ 0 & 1 \end{array} \right]. \quad (\text{A.33})$$

Next, a vector \mathbf{q}_{OUT} will represent the connection of the output current source, which has a 1 in the last position and zeros elsewhere:

$$\mathbf{q}_{OUT} = \left[\begin{array}{cccc} 0 & 0 & 0 & 1 \end{array} \right]. \quad (\text{A.34})$$

Finally, diagonal matrices \mathbf{R} and \mathbf{C} will be defined containing switch on-state resistance and capacitor values, respectively.

A.4.2 Single-Phase Dynamics

The next step is to calculate the dynamics of a single phase network of an SC converter. Section A.4.1 defined the relevant single-phase network matrices used in this section. For simplicity of the explanation, the specific phase superscripts are omitted in this section with the understanding that the appropriate superscripts are used for each phase's dynamics. The converter dynamics are determined by calculating the state vector \mathbf{v} given the system state and output current.

First, the resistive drops of the on-state switches must be determined. If the current through the links is given by \mathbf{i}_L , the currents through the on-state switches can be found using (A.26):

$$\mathbf{i}_r = \mathbf{Q}_{RCx} \mathbf{i}_L. \quad (\text{A.35})$$

Equation (A.35) can then be multiplied by \mathbf{R} to determine the resistive voltage drops, denoted \mathbf{v}_r , across the switches.

The fundamental loop matrix \mathbf{B} determines the voltage around each fundamental loop in the circuit. Since \mathbf{B} only accounts for the input source and capacitor voltages, the error in the KVL equation in A.11 is equal to the switch-related voltage drops in the circuit. The switch-related voltage drops around each fundamental loop in the phase network can be found in terms of the resistive voltage drops \mathbf{v}_r . Since the columns of \mathbf{Q}_{RCx} represent the presence and orientation of each switch in each fundamental loop, it can be used to find the switch-based resistive voltage drop around each fundamental loop:

$$\mathbf{v}_{r,loop} = \mathbf{Q}_{RCx}^\top \mathbf{v}_r. \quad (\text{A.36})$$

This loop voltage can be equated to the loop resistive drops by:

$$\mathbf{B} \mathbf{v} = \mathbf{b}_{IN} V_{IN} + \mathbf{B}_C \mathbf{v}_C = -\mathbf{Q}_{RCx}^\top \mathbf{R} \mathbf{Q}_{RCx} \mathbf{i}_L. \quad (\text{A.37})$$

The link currents can be found directly in terms of the capacitor state and input voltage by solving (A.37) for \mathbf{i}_L :

$$\mathbf{i}_L = -\left(\mathbf{Q}_{RCx}^\top \mathbf{R} \mathbf{Q}_{RCx}\right)^{-1} (\mathbf{B}_C \mathbf{v}_C + \mathbf{b}_{IN} V_{IN}). \quad (\text{A.38})$$

The circuit currents can be found by multiplying the link currents by the transpose of the fundamental loop matrix \mathbf{B} . As the currents in the links represent the currents in each fundamental loop, the transpose of \mathbf{B} is used to find the currents in all capacitors. Since the output current and the output capacitor current are lumped in the last parameter of the state vector, the output voltage must be subtracted from the currents to obtain the capacitor currents as follows:

$$\mathbf{i}_C = -\mathbf{B}_C^\top \left(\mathbf{Q}_{RCx}^\top \mathbf{R} \mathbf{Q}_{RCx}\right)^{-1} (\mathbf{B}_C \mathbf{v}_C + \mathbf{b}_{IN} V_{IN}) - \mathbf{q}_{OUT} I_{OUT}. \quad (\text{A.39})$$

Similarly, the input current is found by using the component \mathbf{b}_{IN} from (A.11):

$$i_{IN} = -\mathbf{b}_{IN}^\top \left(\mathbf{Q}_{RCx}^\top \mathbf{R} \mathbf{Q}_{RCx} \right)^{-1} (\mathbf{B}_C \mathbf{v}_C + \mathbf{b}_{IN} V_{IN}). \quad (\text{A.40})$$

Finally, since the capacitor currents are known, the derivative of the capacitor voltages can be obtained by simply multiplying by the inverse of the capacitance matrix:

$$\dot{\mathbf{v}}_C = -\mathbf{C}^{-1} \left[\mathbf{B}_C^\top \left(\mathbf{Q}_{RCx}^\top \mathbf{R} \mathbf{Q}_{RCx} \right)^{-1} (\mathbf{B}_C \mathbf{v}_C + \mathbf{b}_{IN} V_{IN}) + \mathbf{q}_{OUT} I_{OUT} \right]. \quad (\text{A.41})$$

Now that the defining differential equation for a single phase network of an SC converter has been found, a standard-form linear system will be created from (A.41). The continuous-time standard-form linear system is given in the following form:

$$\dot{\mathbf{v}}_C = \mathbf{A} \mathbf{v}_C + \mathbf{B} \begin{bmatrix} V_{IN} \\ I_{OUT} \end{bmatrix} \quad (\text{A.42})$$

$$\begin{bmatrix} v_{OUT} \\ i_{IN} \end{bmatrix} = \mathbf{C} \mathbf{v}_C + \mathbf{D} \begin{bmatrix} V_{IN} \\ I_{OUT} \end{bmatrix}. \quad (\text{A.43})$$

From (A.39) and (A.40), the following values of \mathbf{A} , \mathbf{B} , \mathbf{C} and \mathbf{D} can be extracted:

$$\mathbf{A} = -\mathbf{C}^{-1} \mathbf{B}_C^\top \left(\mathbf{Q}_{RCx}^\top \mathbf{R} \mathbf{Q}_{RCx} \right)^{-1} \mathbf{B}_C \quad (\text{A.44})$$

$$\mathbf{B} = \begin{bmatrix} -\mathbf{C}^{-1} \mathbf{B}_C^\top \left(\mathbf{Q}_{RCx}^\top \mathbf{R} \mathbf{Q}_{RCx} \right)^{-1} \mathbf{b}_{IN} & -\mathbf{C}^{-1} \mathbf{q}_{OUT} \end{bmatrix} \quad (\text{A.45})$$

$$\mathbf{C} = \begin{bmatrix} \mathbf{q}_{OUT}^\top \\ -\mathbf{b}_{IN}^\top \left(\mathbf{Q}_{RCx}^\top \mathbf{R} \mathbf{Q}_{RCx} \right)^{-1} \mathbf{B}_C \end{bmatrix} \quad (\text{A.46})$$

$$\mathbf{D} = \begin{bmatrix} 0 & 0 \\ -\mathbf{b}_{IN}^\top \left(\mathbf{Q}_{RCx}^\top \mathbf{R} \mathbf{Q}_{RCx} \right)^{-1} \mathbf{b}_{IN} & 0 \end{bmatrix} \quad (\text{A.47})$$

The previous six equations fully describe a linear system describing the dynamics of a single converter clock phase. For any properly-posed two-phase converter, the matrices \mathbf{A}^1 , \mathbf{A}^2 , \mathbf{B}^1 , \mathbf{B}^2 , \mathbf{C}^1 , \mathbf{C}^2 , \mathbf{D}^1 and \mathbf{D}^2 can be formed from the fundamental matrices developed

in section A.2. For the 3:1 ladder converter example, the eight linear system matrices can be found using the following resistor and capacitor matrices, optimized in chapter 3:

$$\mathbf{C} = \begin{bmatrix} 1 & & & \\ & 2 & & \\ & & 1 & \\ & & & 5 \end{bmatrix} \cdot 10^{-6} \quad \mathbf{R} = \begin{bmatrix} .2 & & & \\ & .2 & & \\ & & .2 & \\ & & & .2 \\ & & & & .1 \\ & & & & & .1 \end{bmatrix} \quad (\text{A.48})$$

$$\mathbf{A}^1 = \begin{bmatrix} -3.75 & -2.5 & -1.25 & -3.75 \\ -1.25 & -2.5 & 1.25 & -1.25 \\ -1.25 & 2.5 & -3.75 & -1.25 \\ -0.75 & -0.5 & -0.25 & -0.75 \end{bmatrix} \cdot 10^6, \quad \mathbf{A}^2 = \begin{bmatrix} -3.75 & -2.5 & 3.75 & 2.5 \\ -1.25 & -2.5 & 1.25 & 2.5 \\ 3.75 & 2.5 & -3.75 & -2.5 \\ 0.5 & 1 & -0.5 & -1 \end{bmatrix} \cdot 10^6 \quad (\text{A.49})$$

$$\mathbf{B}^1 = \begin{bmatrix} 3.75 & 0 \\ 1.25 & 0 \\ 1.25 & 0 \\ 0.75 & -0.2 \end{bmatrix} \cdot 10^6, \quad \mathbf{B}^2 = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & -0.2 \end{bmatrix} \cdot 10^6 \quad (\text{A.50})$$

$$\mathbf{C}^1 = \begin{bmatrix} 0 & 0 & 0 & 1 \\ 3.75 & 2.5 & 1.25 & 3.75 \end{bmatrix}, \quad \mathbf{C}^2 = \begin{bmatrix} 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 \end{bmatrix} \quad (\text{A.51})$$

$$\mathbf{D}^1 = \begin{bmatrix} 0 & 0 \\ -3.75 & 0 \end{bmatrix}, \quad \mathbf{D}^2 = \mathbf{0} \quad (\text{A.52})$$

These system parameters can be used to perform a continuous-time simulation of the SC converter using MATLAB's *ode23* or similar ODE solver. While this ODE representation and a SPICE simulation yield identical results, the dimension of the ODE problem is significantly reduced.

A.4.3 Discrete-Time Model

The time-dependent continuous-time linear model for a SC converter, as developed in section A.4.2, is useful for simulating an SC converter. However, for use in converter controllers, a discrete-time model may be more appropriate. The sample time for this discrete-time model is a single switching period, incorporating all n clock phases in sequence.

For purpose of illustration, this analysis will be performed for a single-input, single-output two-phase converter, although it can be extended for a multi-phase converter. A switching period of T is assumed, where each of the two clock phases takes up precisely half of this switching period. The system will be sampled at the instant of time before the phase 2 to phase 1 transition. The capacitor voltage vector at this time is denoted $\mathbf{v}_C[k]$ at sample k . The input voltage and output current of the converter will be considered constant during each switching period, and denoted as $V_{IN}[k]$ and $I_{OUT}[k]$, respectively, for the duration between sample k and sample $k + 1$. Similarly, the output voltage at sample k will be denoted $V_{OUT}[k]$. In the discrete-time system, the input current will be excluded from the system output vector for simplicity.

Let the system state at time kT be $\mathbf{v}_C[k]$. To find $\mathbf{v}_C[k + 1]$, the system must be integrated from time kT to time $(k + 1)T$. First, the system will be integrated using the phase 1 system parameters to time $(k + 1/2)T$. This integration is given by [10] by:

$$\mathbf{v}_C((k + 1/2)T) = e^{\mathbf{A}^1 T/2} \mathbf{v}_C(kT) + \int_0^{T/2} e^{\mathbf{A}^1 (T/2 - \tau)} \mathbf{B}^1 \mathbf{u}(\tau) d\tau \quad (\text{A.53})$$

where $\mathbf{u}(t)$ is the input vector comprising of the input voltage and output current. While (A.53) looks like the solution to a single-variable state integration, it utilizes the matrix exponential, given by the Taylor expansion:

$$e^{\mathbf{A}} = \mathbf{I} + \frac{1}{1!} \mathbf{A} + \frac{1}{2!} \mathbf{A} \mathbf{A} + \frac{1}{3!} \mathbf{A} \mathbf{A} \mathbf{A} + \cdots \quad (\text{A.54})$$

Since $\mathbf{u}(t) = \mathbf{u}[k]$ from $t = kT$ to $t = (k + 1)T$, (A.53) can be simplified as follows:

$$\mathbf{v}_C((k + 1/2)T) = e^{\mathbf{A}^1 T/2} \mathbf{v}_C(kT) + \int_0^{T/2} e^{\mathbf{A}^1 \tau} d\tau \mathbf{B}^1 \mathbf{u}[k]. \quad (\text{A.55})$$

Similarly, if the state $\mathbf{v}_C((k+1/2)T)$ is known, the state at time $(k+1)T$ can be found as follows:

$$\mathbf{v}_C((k+1)T) = e^{\mathbf{A}^2 T/2} \mathbf{v}_C((k+1/2)T) + \int_0^{T/2} e^{\mathbf{A}^2 \tau} d\tau \mathbf{B}^2 \mathbf{u}[k]. \quad (\text{A.56})$$

Now, (A.55) and (A.56) can be combined to find the state sample $k+1$ from the state at sample k :

$$\mathbf{v}_C[k+1] = e^{\mathbf{A}^2 \frac{T}{2}} e^{\mathbf{A}^1 \frac{T}{2}} \mathbf{v}_C[k] + e^{\mathbf{A}^2 \frac{T}{2}} \int_0^{T/2} e^{\mathbf{A}^1 \tau} d\tau \mathbf{B}^1 \mathbf{u}[k] + \int_0^{T/2} e^{\mathbf{A}^2 \tau} d\tau \mathbf{B}^2 \mathbf{u}[k]. \quad (\text{A.57})$$

This definite integral of the matrix exponential above is given by:

$$\int_0^{T/2} e^{\mathbf{A} \tau} d\tau = \frac{T}{2} + \frac{1}{2!} \mathbf{A} \left(\frac{T}{2} \right)^2 + \frac{1}{3!} \mathbf{A}^2 \left(\frac{T}{2} \right)^3 \dots \quad (\text{A.58})$$

Since \mathbf{A} is not necessarily invertible, (A.58) does not necessarily have a closed form.

While (A.57) describes the system, it is useful to put the system in the standard state-space form for a discrete-time linear system. The standard form of a discrete-time system is given by:

$$\mathbf{v}_C[k+1] = \mathbf{A}_D \mathbf{v}_C[k] + \mathbf{B}_D \begin{bmatrix} V_{IN}[k] \\ I_{OUT}[k] \end{bmatrix} \quad (\text{A.59})$$

where the output of the system is given by:

$$V_{OUT}[k] = \mathbf{q}_{OUT}^\top \mathbf{v}_C[k]. \quad (\text{A.60})$$

The discrete-time linear system model parameters \mathbf{A}_D and \mathbf{B}_D can be extracted from (A.57) in terms of the continuous-time system parameters:

$$\mathbf{A}_D = e^{\mathbf{A}^2 \frac{T}{2}} e^{\mathbf{A}^1 \frac{T}{2}} \quad (\text{A.61})$$

$$\mathbf{B}_D = e^{\mathbf{A}^2 \frac{T}{2}} \int_0^{T/2} e^{\mathbf{A}^1 \tau} d\tau \mathbf{B}^1 + \int_0^{T/2} e^{\mathbf{A}^2 \tau} d\tau \mathbf{B}^2. \quad (\text{A.62})$$

The continuous-time system parameters for the 3:1 ladder converter example found in section A.4.2 can be used to find the discrete-time linear system parameters. In this

example, a switching frequency of 1 MHz is used such that $T = 10^{-6}$. The discrete-time system parameters for the ladder converter are given approximately as follows:

$$\mathbf{A}_D = \begin{bmatrix} 0.1276 & -0.0912 & -0.0030 & -0.2889 \\ -0.2023 & 0.2949 & 0.1332 & 0.3628 \\ 0.0519 & 0.1562 & 0.1176 & -0.5316 \\ -0.1242 & 0.0229 & 0.0011 & 0.6498 \end{bmatrix} \quad (\text{A.63})$$

$$\mathbf{B}_D = \begin{bmatrix} 0.4185 & 0.0020 \\ 0.1375 & -0.0725 \\ 0.4020 & 0.0564 \\ 0.1501 & -0.1564 \end{bmatrix} \quad (\text{A.64})$$

The output voltage is simply the last element of the state vector.

The discrete-time linear system found in this section can be used to implement a state-space controller for an SC converter. In addition, once the discrete-time parameters are found, the system can be simulated with very little processor effort.

A.4.4 Dynamics Simulation

The 3:1 ladder converter, shown in figure A.2, is simulated using both the continuous-time time-dependent linear system model, developed in section A.4.2, and the discrete-time time-independent linear system model, developed in section A.4.3. The startup transient of the converter is simulated where the input voltage is a constant 3 volts, the output current a constant 300 mA and each capacitor is initially discharged. A switching frequency of 1 MHz is used.

Figure A.5 plots the four capacitor voltages (where the output capacitor is labeled) using both the continuous-time and discrete-time models. In addition, the results of a SPICE simulation of the ideal converter is overlaid using gray lines. The discrete-time model results are shown as dots for each switching period, matching exactly with the continuous-time model (shown with solid lines). The calculated model matches well with the SPICE

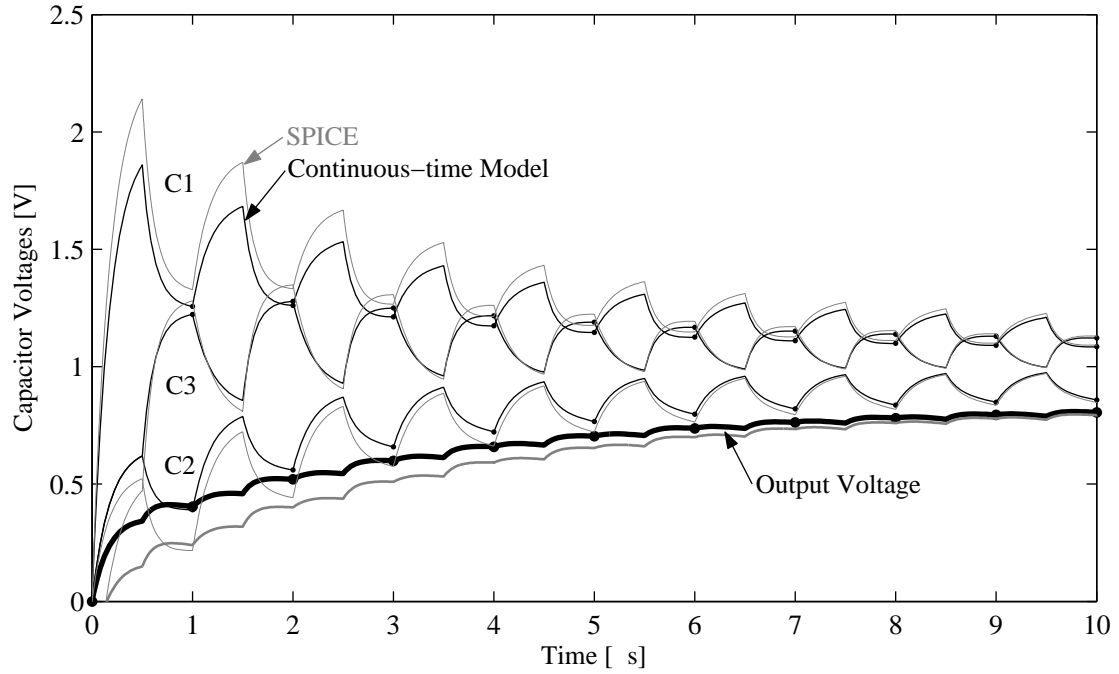


Figure A.5. Simulation of the dynamics of 3:1 ladder converter

simulation; the only difference stems from the difference in initial conditions between the two simulations.

The circuit-theory based dynamic model for SC converter is straightforward to develop from the fundamental matrices describing an SC converter. The linear models can be used to replace SPICE for circuit simulations of ideal SC converters and to create high-performance controllers.

Appendix B

MATLAB Package for Switched-Capacitor Converter Design

Chapters 2, 3 and 4 develop a thorough design methodology for switched-capacitor (SC) DC-DC converters. Designing an SC converter by these methods involve first choosing the correct topology and finding its charge multipliers and matching components with device technologies. Each capacitor and switch is then sized relative to the other capacitors and switches, respectively. Finally, the total switch area, switching frequency and capacitor area must be chosen to optimize performance. Automating this many-step process is strongly desirable in order to speed up the design process. Additionally, computer-based visualization is an important part of the design process as seen in chapters 3 and 8. This appendix describes (and gives source listings for) a set of MATLAB programs that automate the design and optimization of an SC converter. This package has been used to generate many of the contour and regulation efficiency plots in this work. The first section describes the functions which form the backbone of the analysis, including functions to formulate topologies, assign device technologies to specific components in the technologies, and evaluate the loss for

an implemented topology for specific operating conditions. The second section discusses functions which perform certain analyses on SC topologies. The third section includes functions which are utilitarian in nature and used with other functions, followed by a section describing how to use the package for a practical example. Finally, source listings of all the functions are given.¹

B.1 Core Functions

The three functions in this section, `generate_topology`, `implement_topology` and `evaluate_loss`, form the core of the design package. These functions respectively specify the idealized topology structure, assign and size devices for each component, and evaluate the loss of the converter at a certain operating point.

The first function, `generate_topology`, takes a string descriptor of a topology type (given in section 4.2) and a conversion ratio, and creates a topology data structure specifying the properties of the topology. The charge multipliers and blocking voltages are generated based on the formulas in section 4.2. The function is given by:

```
topology = generate_topology (topology_name, num [, denom])
```

<code>topology_name</code>	a quoted name of the SC topology (i.e. 'Series-Parallel', 'Ladder')
<code>num</code>	a decimal version of the step-up ratio of the converter. Must be a rational number
<code>denom</code>	nominal output voltage of the converter. If this parameter is included, <code>num</code> must be an integer, and the conversion ratio is equal to <code>num/denom</code> .
<code>topology</code>	returns a structure containing the charge multipliers and voltages of the individual components in the converter

The output structure, `topology`, has the following members:

¹The source code is provided digitally at <http://www.mikeseeman.com/thesis>.

topName	a quoted name of the SC topology (i.e. 'Series-Parallel', 'Ladder'), as provided by generate_topology
ac	a row vector containing the charge multiplier for each capacitor (not including the output source)
vc	a row vector containing the nominal blocking voltages for each capacitor
vcb	a row vector containing the nominal amplitude of the voltage ripple on the bottom plate parasitic of each capacitor
ar	a row vector containing the charge multiplier for each switch
vr	a row vector containing the nominal blocking voltage of each switch
vrb	a row vector containing the nominal amplitude of the voltage ripple on the source-substrate capacitance of each switch
Mssl	the idealized slow-switching-limit converter metric, given in (4.5)
Mfsl	the idealized fast-switching-limit converter metric, given in (4.6)
ratio	the nominal conversion ratio of the converter (greater than one for a step-up converter)

This **topology** structure is fed into the function **implement_topology** to choose and size devices to implement each component in the topology. The function is used as follows:

```
implementation = implement_topology (topology, Vin, switchTechs, capTechs,
                                     compMetric)
```

topology	topology structure, generated from generate_topology
Vin	maximum input voltage of converter, used for component voltage compatibility
switchTechs	a row vector of switch technology structures that are available for component implementation. A description of this structure follows.
capTechs	a row vector of capacitor technology structures that are available for component implementation. A description of this structure follows.

<code>compMetric</code>	an integer specifying which metric to use when selecting switch technologies. 1 (default) specifies the area-based metric, while 2 selects the parasitic-loss-based metric.
<code>implementation</code>	returns a structure containing the technology structures for the selected devices, plus the relative sizing of each device.

The `implementation` structure returned by `implement_topology` contains the following members:

<code>topology</code>	the structure generated by <code>generate_topology</code> , passed to <code>implement_topology</code>
<code>capacitors</code>	a row vector containing the capacitor technology structure for each capacitor in the converter
<code>switches</code>	a row vector containing the switch technology structure for each switch in the converter
<code>cap_size</code>	a row vector containing the relative sizes of each capacitor in the converter. If this vector was multiplied by the size of each technology-dependent unit cell, the total capacitor area would equal one square meter.
<code>switch_size</code>	a row vector containing the relative sizes of each switch in the converter. If this vector was multiplied by the size of each technology-dependent unit cell, the total switch area would equal one square meter.

The technology structures are contained in a library file, and executed before running `implement_topology`. The *techlib.m* file includes the structures for the ITRS-based idealized devices discussed in section 8.1. Each structure is devoted to a single device in a specific technology. Any number of these structures can be applied to `implement_topology` to choose for implementing a topology. Each structure contains data on an arbitrarily-sized representative unit cell. The capacitor structure has the following members:

<code>tech_name</code>	a string describing the process technology (i.e. ITRS 90nm)
------------------------	---

dev_name	a string describing the particular device (i.e. Thin-oxide PMOS oxide capacitor)
capacitance	The capacitance (in F) of the unit cell device
area	The die area, increased by any density rules, of the unit cell device (in m ²)
bottom_cap	The bottom-plate parasitic capacitance of the unit cell device (in F)
esr	The equivalent series resistance (ESR) of the unit cell device (in ohms)
rating	The maximum blocking voltage of the capacitor (in V)

Similarly, the switch technology structure has the following elements:

tech_name	a string describing the process technology (i.e. ITRS 90nm)
dev_name	a string describing the particular device (i.e. Native 90nm NMOS transistor)
area	The die area of the unit-cell switch, accounting for density rules (in m ²)
conductance	The conductance of the unit-cell switch, at very low V_{DS} and full V_{GS} (in S)
gate_rating	The nominal gate drive voltage of the switch (at which the conductance was measured) (in V)
drain_rating	The maximum blocking voltage of the device (in V)
gate_cap	The average gate capacitance of the unit cell at the rated gate voltage (in F)
drain_cap	The average drain capacitance of the unit cell at the nominal blocking voltage (in F)
body_cap	The linearized source-substrate capacitance of the unit cell at an average source-substrate voltage (in F)

To evaluate the loss of an implemented converter, a flexible approach must be taken.

When investigating the design space with a contour plot, as in section 3.3.2, the output voltage is not constrained (it is a dependent or endogenous variable). However, when regulation is considered, the switching frequency is instead unconstrained. The function `evaluate_loss` takes all system parameters as an input; unspecified ones should be passed as an empty array (`[]`). All inputs, except for the implementation structure, can be either a scalar, row vector, column vector or matrix. Each is internally expanded into a matrix with a two-dimensional parameter space, according to the inputs. At each point, the unspecified (endogenous) variables are found and the converter loss is found.

```
performance = evaluate_loss (imp, Vin, Vout, Iout, fsw, Asw, Ac)
```

<code>imp</code>	implementation structure for a single topology, generated from <code>implement_topology</code>
<code>Vin</code>	input voltage to the converter (in V)
<code>Vout</code>	converter output voltage (in V), set to <code>[]</code> for unregulated converters
<code>Iout</code>	output current (in A)
<code>fsw</code>	converter switching frequency (in Hz), set to <code>[]</code> for regulated converters
<code>Asw</code>	switch die area (in m ²)
<code>Ac</code>	capacitor die area (in m ²)

`evaluate_loss` returns a single data structure denoted `performance`. Each of the following members is a matrix the size of the input parameter range. Each matrix element is the result of evaluating the converter at the specific operating condition.

<code>Vout</code>	the actual average output voltage of the converter. If <code>Vout</code> is specified, it is not changed.
<code>fsw</code>	the actual switching frequency of the converter. If <code>fsw</code> is specified, it is not changed.

<code>is_possible</code>	a matrix where each element is 0 or 1. 1 indicates that the output voltage can be produced for a finite switching frequency; 0 indicates that no solution exists for the input conditions. When output voltage is unconstrained, as in the unregulated case, <code>is_possible</code> is always 1.
<code>efficiency</code>	numerical efficiency of the converter, does not exceed 1
<code>total_loss</code>	the total power dissipated in the converter (in W)
<code>impedance</code>	total output-referred impedance (in ohms)
<code>dominant_loss</code>	a code indicating the dominant loss component at the current design point
<code>dominant_text</code>	a string referring to the dominant loss component at the current design point

These three functions perform the backbone of the analysis functions in the next section. The code listings for the previous sections are in section B.5

B.2 Visualization Functions

Two functions are included in the package which use the functions in section B.1 to create plots which aid in the development of SC converters. The first function, `plot_opt_contour`, plots an efficiency contour plot over a two-dimensional space of switching frequency and switch area for a given input voltage and output current. The second function, `plot_regulation` plots the efficiency of one or more SC converter topologies as either the input or output voltage is swept across a range while the other is held constant. Regulation is performed by varying switching frequency.

```
plot_opt_contour (topology, ratio, Vin, Iout, Ac, switches, capacitors,
                  [esr, [optMethod, [pointPlots, [plotAxes]]]])
```

<code>topology</code>	A string naming the SC topology used (i.e. 'Ladder') or a topology or implementation structure
<code>ratio</code>	A rational conversion ratio for the topology named in <code>topology</code> . This parameter is ignored if <code>topology</code> is a structure
<code>Vin</code>	The scalar input voltage for the converter (in V)
<code>Iout</code>	The scalar output current of the converter (in A)
<code>Ac</code>	The scalar total die area used for the capacitors (in m ²)
<code>switches</code>	A row vector of switch technology structures; see <code>implement_topology</code> . When an implementation structure is passed into <code>topology</code> , this value can be [].
<code>capacitors</code>	A row vector of capacitor technology structures; see <code>implement_topology</code>
<code>esr</code>	Additional metal-related series resistance to add to the analysis (default = 0 ohms)
<code>optMethod</code>	an integer specifying which metric to use when selecting switch technologies. 1 (default) specifies the area-based metric, while 2 selects the parasitic-loss-based metric.
<code>plotPoints</code>	an integer specifying the number of plots in each dimension to evaluate the loss to create the contour plot. A larger number results in smoother contours (default: 100)
<code>plotAxes</code>	A four-element row vector specifying the desired plot axes (calculated automatically by default). It is in the form $[log_{10}(f_{sw,min}), log_{10}(f_{sw,max}), log_{10}(A_{SW,min}), log_{10}(A_{SW,max})]$, where switching frequency is in Hz and switch area in m ² .

An example using `plot_opt_contour` and `plot_regulation` is given in section B.4. Function `plot_regulation` is given by:

```
plot_regulation (topologies, Vin, Vout, Iout, Ac, switches, capacitors,
```


[esr, [idesign]])

topologies	A column vector of topologies to be evaluated over regulation. Each element can either be a two-element row vector in the form [<code>'Topology'</code> {ratio}], a topology structure or implementation structure.
Vin	Input voltage, either a scalar or vector (in V)
Vout	Output voltage, either a scalar or vector (in V)
Iout	Output current, either as a scalar for constant output currents, or as a vector if the load current varies with either load or line voltage (in A)
Ac	The scalar total die area used for the capacitors (in m ²)
switches	A row vector of switch technology structures; see <code>implement_topology</code>
capacitors	A row vector of capacitor technology structures; see <code>implement_topology</code>
esr	Additional metal-related series resistance to add to the analysis (default = 0 ohms)
idesign	A row vector (each element corresponding to a topology) or scalar specifying the current for which each topology should be optimized for (in A). If omitted, idesign is chosen automatically by interpolating the output current at the nominal conversion ratio.

`plot_regulation` plots the efficiency of a number of topologies over a range of either input or output voltages. Either the input or output voltage should be specified as a vector of sample points; this is used as the x-axis for the plot. The ratios according to each converter are noted next to the optimal point of each converter. The sizing of each topology is optimized independently for the nominal operating point. This optimization may not ideally represent an actual converter.

B.3 Helper Functions

Two helper functions are included to perform utilitarian tasks. Function `optimize_loss` is used by `plot_opt_contour` and `plot_regulation` for finding the most-efficient operating point for a given input voltage and output current. Function `permute_topologies` combines sets of topologies in cascade to form new hybrid topologies for use with the other functions. These functions are described as follows.

```
[performance, fsw, Asw] = optimize_loss (implementation, Vin, Iout, Ac)
```

implementation an implementation structure created by `implement_topology` or similar method

Vin the scalar input voltage for the optimization (in V)

Iout the scalar output current for optimization (in A)

Ac the scalar capacitor die area (in m²)

performance the performance structure, as returned by `evaluate_loss`, at the optimal point

fsw the optimal switching frequency (in Hz)

Asw the optimal switch die area (in m²)

```
newtops = permute_topologies (topologies1, topologies2)
```

topologies1 A column vector of m [{'Topology'} {ratio}] pairs or topology structures, each representing a topology that can be used in the first position (attached to the input source)

topologies2 A column vector of n [{'Topology'} {ratio}] pairs or topology structures, each representing a topology that can be used in the second position (attached to the output of the first topology and supplies the output source)

newtops A column vector of length $m \cdot n$ containing topology structures, all combinations of the first topologies and second topologies are included

Function `permute_topologies` cascades two converters, each of which can be a variable-ratio converter, into a larger variable-ratio converter, such as the converter in section 5.4, representing all of the possible combinations. The resulting vector can be used with `plot_regulation` to obtain a regulation curve for the variable-ratio converter.

B.4 Example

The two-stage variable-ratio SC converter discussed in section 5.4 will be used to demonstrate the abilities of this package. Before any of the following code is run, the script containing the technology structures (*techlib.m*) should be run to load these structures into memory. This example will use the 65 nm process example from the ITRS roadmap. First, the vectors with the first and second stage topologies will be defined:

```
topologies1 = [ generate_topology('Ladder', 8, 7);
                generate_topology('Ladder', 7, 7);
                generate_topology('Ladder', 6, 7);
                generate_topology('Ladder', 5, 7) ];
topologies2 = [ {'Dickson'} {1/3};
                {'Dickson'} {1/2} ];
```

Note the two methods of defining the topology vectors; either works for the methods in this section. It is important to note that the arrangement of capacitors in the ladder topologies is not optimal for this application. Superior performance can be obtained by creating topology structures with the charge multipliers and blocking voltages from the optimized topologies.

Next, the two topology vectors will be cascaded and permuted:

```
cascaded_tops = permute_topologies (topologies1, topologies2);
```

As one of the switches in the Dickson converter must block twice the output voltage (of 1.2V), a cascode device will be created. It consists of two native NMOS devices in series, used to block twice the voltage. Additionally, a high-voltage capacitor will be created (usually, a thick-oxide device would be used, in this case, a series device would be used solely for analysis purposes).

```
itrs65cc = itrs65n; % copy topologies
itrs65cc.area = itrs65n.area * 2;
itrs65cc.conductance = itrs65n.conductance / 2;
itrs65cc.drain_rating = itrs65n.drain_rating * 2;
itrs65cc.drain_cap = itrs65n.drain_cap * 2 + itrs65n.gate_cap;

thickcap = itrs65cap;
thickcap.capacitance = itrs65cap.capacitance / 2;
thickcap.area = itrs65cap.area * 2;
thickcap.rating = itrs65cap.rating * 2;
```

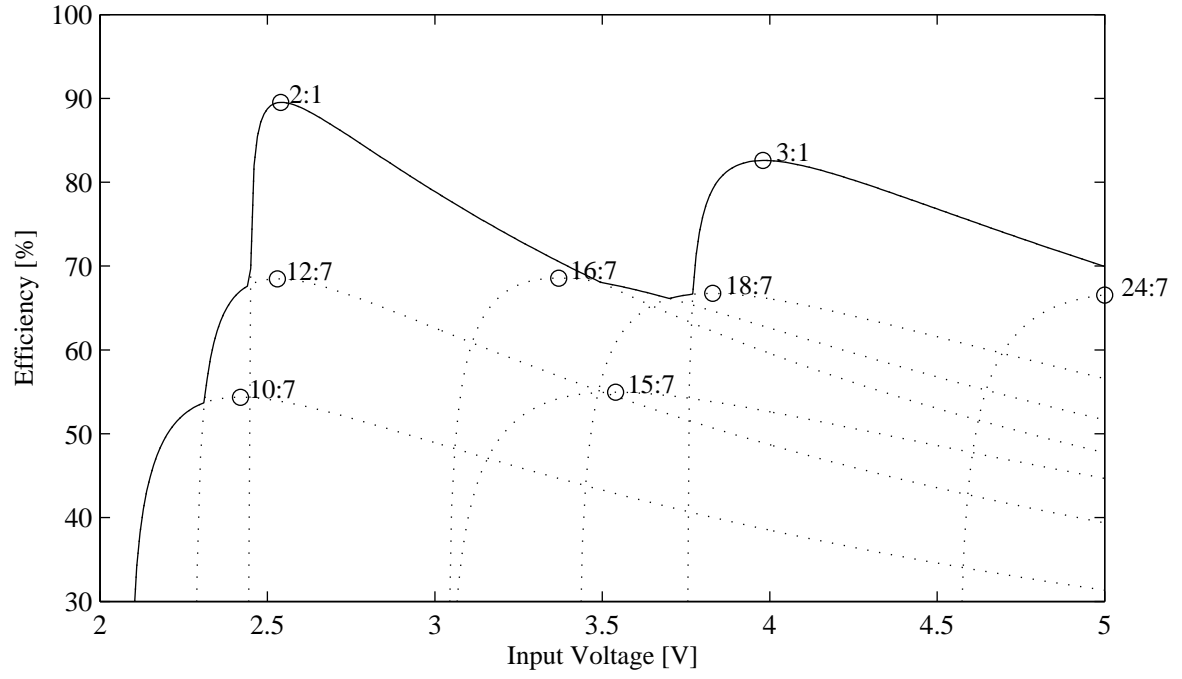
Using these new devices, the regulation efficiency plot can be created. The input voltage is swept from 2 V to 5 V at an output current of 100 mA and a capacitor die area of 10 mm². Again, it is important to note that the arrangement of capacitors in the ladder topologies is not optimal for this application. Superior performance can be obtained by creating topology structures with the charge multipliers and blocking voltages from the optimized topologies. The result from `plot_regulation` is shown in figure B.1a.

```
Vin = 2:.01:5;
plot_regulation (cascaded_tops, Vin, 1.2, 0.1, 10e-6, ...
                 [itrs65n itrs65cc], [itrs65cap thickcap]);
```

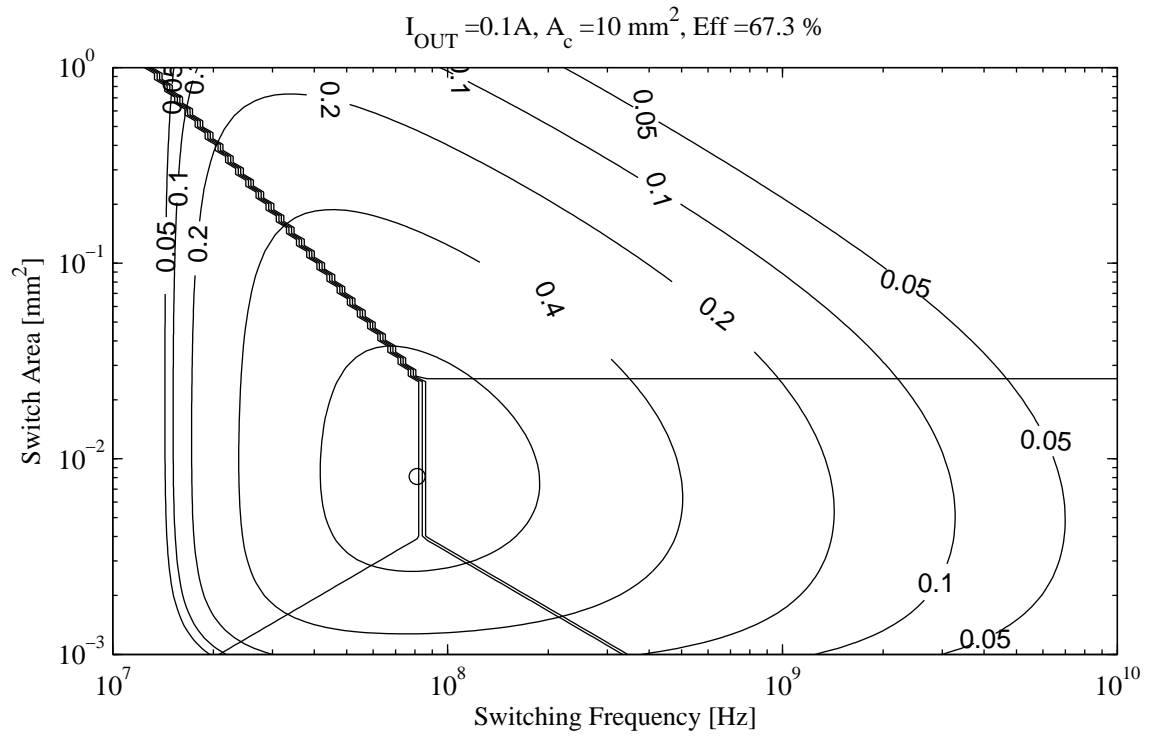
Next, the design point of the 16:7 configuration will be examined. First, this topology structure will be created:

```
topology = permute_topologies( [generate_topology('Ladder', 7, 8)], ...
                               [generate_topology('Dickson', 1/2)]]);
```

Next, the contour plot will be created using the same modified devices as shown above. An input voltage of 3.35 V will be used, as it is close to the optimal point on the previous plot. The optional axis parameter is used to better-center the plot. The results of `plot_opt_contour` are shown in figure B.1b.



(a) plot_regulation



(b) plot_opt_contour

Figure B.1. Example plots from the MATLAB package

```
plot_opt_contour (topology, 1, 3.35, 0.1, 10e-6, [itrs65n itrs65cc], ...  
                  [itrs65cap thickcap], 0, 1, 100, [7 10 -9 -6]);
```

This MATLAB package enables quick design and application space investigation using SC converters. The efficiency of a converter can be estimated in very little time, and the design can be rapidly iterated to achieve the best architecture for a given application. However, as many approximations are used in the analysis, device-level circuit simulations (e.g. SPICE) are necessary for a more-precise estimate of efficiency.

B.5 Code Listings

The source code is provided digitally at <http://www.mikeseeman.com/thesis>.

B.5.1 evaluate_loss.m

```
1  function performance = evaluate_loss (imp, Vin, Vout, Iout, fsw, Asw, Ac)
    % evaluate_loss: evaluates the loss and other performance metrics for a
    % specific size and operating condition of a implemented SC converter
    %
5  %   imp: implementation generated from implement_topology
    %   Vin: converter input voltage for this calc [V]
    %   Vout: converter output voltage for this calc [V]
    %   Iout: converter output current for this calc [A]
    %   fsw: switching frequency [Hz]
10  %   Asw: switch area [m^2]
    %   Ac: capacitor area [m^2]
    %
    %   Either fsw (in case of regulation) or Vout (in case of open-loop
    %   control) should be set to [] and will be found by this function.
15  %
    %   Created: 4/15/08, Last Modified: 4/15/09
    %   Copyright 2008-2009, Mike Seeman, UC Berkeley
    %   May be freely used and modified but never sold. The original author
    %   must be cited in all derivative work.
20
    % Break implementation into components for brevity
    ac = imp.topology.ac;
    vc = imp.topology.vc;
    vcb = imp.topology.vcb;
25  ar = imp.topology.ar;
    vr = imp.topology.vr;
    vrb = imp.topology.vrb;
    ratio = imp.topology.ratio;

30  caps = imp.capacitors;
    cap_size = imp.cap_size;
    switches = imp.switches;
    sw_size = imp.switch_size;

35  % Process (and expand) input parameters
    paramdim = max(size(Vin), max(size(Vout), max(size(Iout), max(size(fsw),...
        max(size(Asw), size(Ac))))));
    type = 0; % undefined: 0-not yet set; 1-vout; 2-fsw

40  Vin = expand_input(Vin, paramdim);
    if (size(Vout) == [0 0])
        type = 1;
        Vout = zeros(paramdim);
    else
```

```

45     Vout = expand_input(Vout, paramdim);
    end
    Iout = expand_input(Iout, paramdim);
    if (size(fsw) == [0 0])
        if (type == 1)
50         error('Both fsw and Vout cannot be undefined');
        else
            type = 2;
            fsw = zeros(paramdim);
        end
55     else
        fsw = expand_input(fsw, paramdim);
        end
        Asw = expand_input(Asw, paramdim);
        Ac = expand_input(Ac, paramdim);
60     %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% Start Analysis %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
        % Calculate SSL output resistance:

        Rssl_alpha = 0;
65     for i=1:size(caps,2),
        if (ac(i) > 0),
            Rssl_alpha = Rssl_alpha + (ac(i)^2)/(caps(i).capacitance*cap_size(i));
        end
    end
70     % Calculate FSL output resistance:

    Rfsl_alpha = 0;
    for i=1:size(switches,2),
75     if (ar(i) > 0),
        Rfsl_alpha = Rfsl_alpha + 2*(ar(i)^2)/...
            (switches(i).conductance*sw_size(i));
        end
    end
80     Rfsl = Rfsl_alpha./Asw;

    % Calculate additional ESR loss:
    Resr_alpha = 0;
    for i=1:size(caps,2),
85     if (isfield(caps(i), 'esr')),
        if (ac(i) > 0),
            Resr_alpha = Resr_alpha + 4*(ac(i)^2)*(caps(i).esr/cap_size(i));
        end
    end
90     end
    Resr = Resr_alpha./Ac;
    if (isfield(imp, 'esr')),
        Resr = Resr + imp.esr;
    end
95     % Find the unknown (endogenous) variable
    if (type == 1)

```



```

    % Vout is unknown
    Rssl = Rssl_alpha ./ (fsw.*Ac);
100
    % Calculate total output resistance:
    Rout = sqrt(Rssl.^2 + (Rfsl + Resr).^2);
    Vout = Vin*ratio - Rout.*Iout;
    Pout = Vout.*Iout;
105    is_prac = ones(paramdim);
elseif (type == 2)
    % fsw is unknown
    % Calculate needed output impedance and switching frequency to match
    % output voltage
110    % is_prac is 1 if a finite fsw which satisfies Iout, Vin, Vout exists

    Rreq = (Vin*ratio - Vout)./Iout;
    is_prac = ((Rreq > 0) & (Rfsl+Resr < Rreq));
    Rssl = real(sqrt(Rreq.^2 - (Rfsl+Resr).^2));
115    fsw = Rssl_alpha ./ (Rssl .* Ac);

    % Calculate total output resistance:
    Rout = sqrt(Rssl.^2 + (Rfsl + Resr).^2);
    Pout = Vout.*Iout;
120 else
    error('Either Vout or fsw must be []');
end

% Calculate resistance losses:
125 Pssl = Rssl.*Iout.^2;
    Pfsl = Rfsl.*Iout.^2;
    Pesr = Resr.*Iout.^2;
    Pres = Rout.*Iout.^2;

130 % Calculate Cap-related Parasitic loss:

    Pc_alpha = 0;
    for i=1:size(caps,2),
        Pc_alpha = Pc_alpha + (caps(i).bottom_cap*cap_size(i)) * (vcb(i))^2;
135    end
    Pc = Pc_alpha.*fsw.*Ac.*Vin.^2;

    % Calculate Switch-related Parasitic loss:

140    Psw_alpha = 0;
    Pg_alpha = 0;
    for i=1:size(switches,2),
        % Assume switch is driven at full gate_rating voltage
        Vgssw = switches(i).gate_rating;
145        Pg_alpha = Pg_alpha + (switches(i).gate_cap*sw_size(i)) * (Vgssw)^2;
        Psw_alpha = Psw_alpha + ((switches(i).drain_cap*sw_size(i)) * (vr(i))^2 + ...
                                (switches(i).body_cap*sw_size(i)) * (vrb(i))^2);
    end
    Psw = (Psw_alpha.*Vin.^2 + Pg_alpha).*fsw.*Asw;
150

```

```

% Calculate total loss, efficiency, etc...
Ploss = Pres + Pc + Psw;
eff = Pout./(Pout+Ploss);
IND = [];
155 for i=1:size(Pssl,1),
    [temp, ind] = max([Pssl(i,:); Pfs1(i,:); Pesr(i,:); Pc(i,:); Psw(i,:)]);
    IND = [IND; ind];
end
%[temp, ind] = max([Pssl Pfs1 Pc Psw]);
160 texts = [{'SSL Loss'} {'FSL Loss'} {'ESR Loss'} {'Bottom-Plate'}...
    {'Switch Parasitic'}];

% create structure -- list unknown system parameters
performance.Vout = Vout;
165 performance.fsw = fsw;
performance.is_possible = is_prac;

% list performance
performance.efficiency = eff;
170 performance.total_loss = Ploss;
performance.impedance = Rout;
performance.dominant_loss = IND;
performance.dominant_text = texts(IND);

175 % Sub-function that turns input into a (maxsize) matrix
function result = expand_input (input, maxsize)

if (size(input) == [1 1])
    % scalar input
180 result = input * ones(maxsize);
elseif (size(input) == [1 maxsize(2)])
    % row vector input
    result = ones(maxsize(1),1) * input;
elseif (size(input) == [maxsize(1) 1])
185 % column vector input
    result = input * ones(1, maxsize(2));
elseif (size(input) == maxsize)
    % input already a properly-sized matrix
    result = input;
190 elseif (size(input) == [0 0])
    error('Only fsw or Vout can be empty');
    result = 0;
else
    % input is not properly sized
195 error('All inputs must have the same number of rows and columns (if not 1)');
    result = 0;
end

```

B.5.2 generate_topology.m

```

1 function result = generate_topology (topology_name, num, den)

```

```

% generate_topology: Topology charge and voltage multiplier generation
%
% result = generate_topology (topology_name, num [, den])
5 % topology_name: Name of SC topology {Ladder, Dickson, Cockcroft-Walton,
% Doubler, Series-Parallel, Fibonacci}
% num, den: the ratio of output voltage to input voltage. If denom is
% omitted, num is a rational number. Otherwise, both are integers.
% num/den is the step-up conversion ratio of the converter.
10 %
% result: structure with charge multiplier and voltage vectors for
% capacitors and switches.
%
% Created 4/14/08, Last Modified 4/15/09
15 % Copyright 2008-2009, Mike Seeman, UC Berkeley
% May be freely used and modified but never sold. The original author
% must be cited in all derivative work.

% if a straight ratio passed in, break it up into numerator and denominator
20 if nargin < 3,
    [num, den] = rat(num, .001);
end

% generate ac's for step-up only, at first, v's in terms of input voltage
25 flip = 0;
if (num/den < 1),
    t = den; den = num; num = t;
    flip = 1; % indicate that the converter has been 'flipped'
end

30 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% Series-Parallel %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
if (strcmpi(topology_name, 'Series-Parallel')),
    n = num;
    m = den;
35 N = n;
% SSL values
ac = ones(1, m*(n-m))/m;
vc = ones(1, m*(n-m))/m;
vcb = [];
40 for i=1:m,
    for j=1:(n-m),
        vcb = [vcb (i+j-1)/m];
    end
end
% FSL values
45 vr = [];
vrb = [];
for i = 1:m,
    for j = 1:(n-m+1),
50 if (j == 1),
        vr = [vr i/m];
        vrb = [vrb (i+j-1)/m];
    elseif (j == (n-m+1)),
        vr = [vr (n-m-1+i)/m];
    end
end

```

```

55         vrb = [vrb (i+j-2)/m];
           else
               vr = [vr 1/m];
               vrb = [vrb (i+j-1)/m];
           end
60     end
    end
    for i=1:m+1,
        for j=1:n-m,
            if (i==1),
15         vr = [vr j/m];
            elseif (i==(m+1)),
                vr = [vr (m-1+j)/m];
            else
20         vr = [vr 1/m];
            end
            if ((i==1) || (i==(m+1))),
                vrb = [vrb 0];
            else
30         vrb = [vrb (i+j-2)/m];
            end
75     end
        end
    end
    ar = ones(size(vr))/m;

80 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% Ladder %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    elseif (strcmpi(topology_name,'Ladder')),
        n = num;
        m = den;
        N = n;
85    % SSL values
        ac = [];
        vc = [];
        vcb = [];

90    for j=1:(n-m-1),
        ac = [ac j j];
        vc = [vc 1/m 1/m];
        vcb = [vcb 1/m 0];
    end
95    ac = [ac (n-m)];
    vc = [vc 1/m];
    vcb = [vcb 1/m];
    for j=(m-1):-1:1,
        ac = [ac ones(1,2)*(j*(n/m-1))];
100    vc = [vc 1/m 1/m];
        vcb = [vcb 1/m 0];
    end

    % FSL values
105    ar = [ones(1,2*(n-m)) (n/m-1)*ones(1,2*m)];
    vr = ones(1,2*n)/m;
    vrb = mod(0:(2*n-1),2)/m;

```

```

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% Dickson %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
110 elseif (strcmpi(topology_name,'Dickson')),
    if (den ~= 1)
        error('SWITCHCAP:nonIntegerRatio',...
            'the Dickson topology supports integer ratios only');
    end
115     N = num;
    % SSL values
    ac = ones(1,N-1);
    vc = [];
    vcb = ones(1,N-1);
120     for j=1:(N-1),
        vc = [vc j];
    end
    % FSL values
    if (N == 2),
125         vr = ones(1,4);
        ar = ones(1,4);
        vrb = [0 1 0 1];
    else,
        vr = [ones(1,5) 2*ones(1,N-2), 1];
130         ar = [floor((j+1)/2)*[1 1] floor((j)/2)*[1 1] ones(1,N)];
        vrb = [0 1 0 1 ones(1,N)];
    end

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% Cockcroft-Walton %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
135 elseif (strcmpi(topology_name, 'Cockcroft-Walton')),
    if (den ~= 1)
        error('SWITCHCAP:nonIntegerRatio',...
            'the Cockcroft-Walton topology supports integer ratios only');
    end
140     N = num;
    % SSL values
    ac = [];
    vc = [1 2*ones(1,N-2)];
    vcb = ones(1,N-1);
145     for j=1:(N-1),
        ac = [floor((j+1)/2) ac];
    end
    % FSL values
    if (N == 2),
150         vr = ones(1,4);
        ar = ones(1,4);
        vrb = [0 1 0 1];
    else,
        vr = [ones(1,5) 2*ones(1,N-2) 1];
155         ar = [floor((j+1)/2)*[1 1] floor((j)/2)*[1 1] ones(1,N)];
        vrb = [0 1 0 1 ones(1,N)];
    end

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% Doubler %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
160 elseif (strcmpi(topology_name,'Doubler')),

```

```

    if (den ~= 1)
        error('SWITCHCAP:nonIntegerRatio',...
            'the Doubler topology supports integer ratios only');
    end
165     n = ceil(log2(num));
        N = 2^n;
    if (N ~= num),
        error('SWITCHCAP:badRatio',...
            'the doubler topology supports conversion ratios ~ 2^n');
170     end

    % SSL values
    ac = [];
    vc = [];
175     vcb = [];
    for j=1:(2*n-1),
        ac = [2^floor((j-1)/2) ac];
        vc = [vc 2^floor(j/2)];
        vcb = [vcb 2^floor(j/2)*mod(j,2)];
180     end
    % FSL values
    ar = [];
    vr = [];
    vrb = [];
185     for j=1:n,
        ar = [ar ones(1,4)*2^(j-1)];
        vr = [vr ones(1,4)*2^(n-j)];
        vrb = [vrb [0 1 0 1]*2^(n-j)];
    end
190     %%%%%%%%%%%%%%% Fibonacci %%%%%%%%%%%%%%%
elseif (strcmpi(topology_name,'Fibonacci')),
    if (den ~= 1)
        error('SWITCHCAP:nonIntegerRatio',...
195         'the Fibonacci topology supports integer ratios only');
    end
    i = 2;
    while (fibfun(i) < num),
        i = i+1;
200     end
    if (fibfun(i) > num)
        error('SWITCHCAP:badRatio',...
            'the fibonacci topology supports ratios of F_n or 1/F_n only');
    end
205     N = fibfun(i);

    % SSL Calculation
    ac = [];
    vc = [];
210     vcb = [];
    for j = 2:i-1,
        ac = [fibfun(j-1) ac];
        vc = [vc fibfun(j)];

```

```

        vcb = [vcb fibfun(j-1)];
215     end
        % FSL Calculation
        ar = [1];
        vr = [];
        vrb = [0];
220     for j = 2:i-1,
            ar = [fibfun(j) fibfun(j-1) fibfun(j-1) ar];
            vr = [vr fibfun(j) fibfun(j) fibfun(j-1)];
            vrb = [vrb fibfun(j-1) 0 fibfun(j-1)];
        end
225     vr = [vr fibfun(i-2)];
    end

    ratio = num/den;

230    % Compute ideal metrics
    Mssl = 2*ratio^2/(ac*vc')^2;
    Mfsl = ratio^2/(2*(ar*vr')^2);

    if (flip == 1),
235        ac = ac/ratio;
        vc = vc/ratio;
        vcb = vcb/ratio;
        ar = ar/ratio;
        vr = vr/ratio;
240        vrb = vrb/ratio;
        ratio = 1/ratio;
    end

    result.topName = topology_name;
245    result.ac = ac;
    result.vc = vc;
    result.vcb = vcb;          % bottom plate voltage vector
    result.ar = ar;
    result.vr = vr;
250    result.vrb = vrb;        % body swing voltage, for NMOS
    result.Mssl = Mssl;
    result.Mfsl = Mfsl;
    result.ratio = ratio;

```

B.5.3 implement_topology.m

```

1  function implementation = implement_topology(topology, Vin, switchTechs,...
    capTechs, compMetric)
    % implement_topology: matches components with switches and components in
    % the topology.
5  % implementation = implement_topology(topology, Vin, switchTechs,
    %     capTechs, compMetric)
    % topology: structure created by generate_topology
    % Vin: input voltage of converter

```

```

% switchTechs: an array of technology structures available for switch use
10 % capTechs: an array of technology structures available for cap use
% compMetric: a metric (1=area, 2=loss) used for determining the best
%           component (1=default)
% Created 4/15/08, Last Modified: 4/15/09
% Copyright 2008-2009, Mike Seeman, UC Berkeley
15 % May be freely used and modified but never sold. The original author
% must be cited in all derivative work.

% Break out components of topology structure
ratio = topology.ratio;
20 ac = topology.ac;
ar = topology.ar;
vc = topology.vc*Vin;
vr = topology.vr*Vin;
vcb = topology.vcb*Vin;
25 vrb = topology.vrb*Vin;

if (nargin < 5)
    compMetric=1;
end
30
switch_assign = [];
cap_assign = [];
switch_rel_size = [];
cap_rel_size = [];
35
% Assign Capacitors
for i=1:size(ac,2),
    Mc = 0;
    Cc = 0;          % cap cost;
40    for j=1:size(capTechs,2),
        if (vc(i) <= capTechs(j).rating),
            % Cap could work ... let's see if it's good
            % Use area-limited metric, which is usually applicable
            C = capTechs(j).area;
45            M = capTechs(j).capacitance*vc(i)^2/C;
            if (M > Mc)
                if (Mc == 0),
                    cap_assign = [cap_assign capTechs(j)];
                else
50                    cap_assign(i) = capTechs(j);
                end
                Mc = M;
                Cc = C;
            end
60        end
    end
    % check to make sure a suitable device exists
    if (Mc == 0),
        error(strcat('No capacitors meet the voltage requirement of: ',...
70            num2str(vcb(i))));
    end
end

```



```

        % determine relative device size
        if (ac(i) == 0),
            cap_rel_size = [cap_rel_size 0]; % avoid divide by 0
65     else
            cap_rel_size = [cap_rel_size (ac(i)*vc(i))/...
                            (sqrt(Mc)*cap_assign(i).area)];
        end

70     end

% Assign Switches
for i=1:size(ar,2),
75     Msw = 0;
    Csw = 0; % switch cost;
    for j=1:size(switchTechs,2),
        if (vr(i) <= switchTechs(j).drain_rating),
            % Switch could work ... let's see if it's good
80            if (compMetric == 2), % loss metric
                % assume full gate drive
                C = switchTechs(j).gate_cap*switchTechs(j).gate_rating^2 + ...
                    switchTechs(j).drain_cap*vr(i)^2 + ...
                    switchTechs(j).body_cap*vr(i)^2;
85                M = switchTechs(j).conductance*vr(i)^2/C;
            else % area metric
                C = switchTechs(j).area;
                M = switchTechs(j).conductance*vr(i)^2/C;
            end
90            if (M > Msw)
                if (Msw == 0),
                    switch_assign = [switch_assign switchTechs(j)];
                else
                    switch_assign(i) = switchTechs(j);
95                end
                Msw = M;
                Csw = C;
            end
        end
    end
100    end
    % check to make sure a suitable device exists
    if (Msw == 0),
        error(strcat('No switches meet the voltage requirement of: ',...
            num2str(vr(i))));
105    end
    % determine relative device size
    if (ar(i) == 0),
        switch_rel_size = [switch_rel_size 0];
    else
110        if (compMetric == 2),
            switch_rel_size = [switch_rel_size (ar(i)*vr(i))/...
                                (sqrt(Msw)*switch_assign(i).conductance)];
        else
            switch_rel_size = [switch_rel_size (ar(i)*vr(i))/...

```

```

115         (sqrt(Msw)*switch_assign(i).area)];
        end
    end
end

120 % Scale Caps for unit area:

    cap_area = 0;
    for i=1:size(ac,2),
        cap_area = cap_area + cap_rel_size(i)*cap_assign(i).area;
125    end
    cap_size = cap_rel_size./(cap_area+1e-30);

    % Scale Switches for unit area:

130    sw_area = 0;
    for i=1:size(ar,2),
        sw_area = sw_area + switch_rel_size(i)*switch_assign(i).area;
    end
    switch_size = (switch_rel_size.*(sw_area > 0))./(sw_area+(sw_area == 0));
135

    % Create implementation structure
    implementation.topology = topology;
    implementation.capacitors = cap_assign;
    implementation.switches = switch_assign;
140    implementation.cap_size = cap_size;
    implementation.switch_size = switch_size;

```

B.5.4 optimize_loss.m

```

1  function [performance, fsw, Asw] = optimize_loss (implementation, Vin, ...
    Iout, Ac)
    % optimize_loss: Finds the optimal design point for given conditions
    %   Michael Seeman, UC Berkeley
5  %
    %   optimize_loss(implementation, Vout, Iout, Ac)
    %       implementation: implementation generated from implement_topology
    %       Vin: converter input voltage for this calc [V]
    %       Iout: converter output current for this calc [A]
10  %       Ac: capacitor area [m^2]
    %
    %   Returns: performance structure from evaluate_loss and optimal switching
    %   frequency and switch area
    %
15  %   Created 4/14/08, Last modified: 4/15/09
    %   Copyright 2008-2009, Mike Seeman, UC Berkeley
    %   May be freely used and modified but never sold.  The original author
    %   must be cited in all derivative work.

20  options = optimset('fmincon');
    options = optimset(options, 'TolFun', 1e-11, 'MaxIter', 400000, ...

```

```

        'Display', 'off', 'LargeScale', 'off');
    opt_design = fmincon(@evaluate_loss_opt, [10 -10], [], [], [], [], ...
        [1 -100], [100 1], [], options, implementation, Vin, Iout, Ac);
25  fsw = exp(opt_design(1));
    Asw = exp(opt_design(2));
    performance = evaluate_loss(implementation, Vin, [], Iout, fsw, Asw, Ac);

30  %----- Minimization helper function
    function ploss = evaluate_loss_opt (param, implementation, Vin, Iout, Ac)

        p = evaluate_loss (implementation, Vin, [], Iout, exp(param(1)), ...
            exp(param(2)), Ac);
35  ploss = p.total_loss;

```

B.5.5 permute_topologies.m

```

1  function newtops = permute_topologies (topologies1, topologies2)
    % newtops = permute_topologies(topologies1, topologies2)
    %     topologies1, topologies2: column vectors of either topology
    %     structures or [{'Topology Name'} {ratio}] pairs
5  %
    % For two vectors of topologies, returns a vector of topologies
    % consisting of every permutation of topologies in the first vector
    % connected in series (cascaded) with the topologies in the second
    % vector.
10 %
    % Created 10/08, Last modified: 4/15/09
    % Copyright 2008-2009, Mike Seeman, UC Berkeley
    % May be freely used and modified but never sold. The original author
    % must be cited in all derivative work.
15
    newtops = [];

    for m=1:size(topologies1,1),
        for n=1:size(topologies2,1),
20            % returns an (n*m) vector of topology structures
            top1 = topologies1(m,:);
            top2 = topologies2(n,:);
            if ((size(top1,2) == 1) & (size(top2,2) == 1)),
                newtops = [newtops; cascade_topologies(top1, 1, top2, 1)];
25            elseif ((size(top1,2) == 2) & (size(top2,2) == 1)),
                newtops = [newtops; cascade_topologies(cell2mat(top1(1)), ...
                    cell2mat(top1(2)), top2, 1)];
            elseif ((size(top1,2) == 1) & (size(top2,2) == 2)),
                newtops = [newtops; cascade_topologies(top1, 1, ...
30                    cell2mat(top2(1)), cell2mat(top2(2)))];
            elseif ((size(top1,2) == 2) & (size(top2,2) == 2)),
                newtops = [newtops; cascade_topologies(cell2mat(top1(1)), ...
                    cell2mat(top1(2)), cell2mat(top2(1)), ...
                    cell2mat(top2(2)))];

```

```

35         end
        end
    end

    % ----- Helper: cascade_topologies
40    function newtop = cascade_topologies(topology1, ratio1, topology2, ratio2)
    % cascade_topologies: Combine two topologies into a single topology where
    % the two topologies are cascaded in a series fashion where topology1
    % interfaces with the input and topology2 interfaces with the output

45    if (ischar(topology1)),
        topology1 = generate_topology(topology1, ratio1);
    end

    if (ischar(topology2)),
50        topology2 = generate_topology(topology2, ratio2);
    end

    ratio1 = topology1.ratio;
    ratio2 = topology2.ratio;

55    % scale topology2.v* by ratio1, scale topology1.a* by ratio2
    newtop.topName = strcat(topology1.topName, ' -> ', topology2.topName);
    newtop.ac = [topology1.ac.*ratio2 topology2.ac];
    newtop.ar = [topology1.ar.*ratio2 topology2.ar];
60    newtop.vc = [topology1.vc topology2.vc.*ratio1];
    newtop.vcb = [topology1.vcb topology2.vcb.*ratio1];
    newtop.vr = [topology1.vr topology2.vr.*ratio1];
    newtop.vrb = [topology1.vrb topology2.vrb.*ratio1];
    newtop.ratio = topology1.ratio*topology2.ratio;
65    newtop.Mssl = 2*newtop.ratio^2/(newtop.ac*newtop.vc')^2;
    newtop.Mfsl = newtop.ratio^2/(2*(newtop.ar*newtop.vr')^2);

```

B.5.6 plot_opt_contour.m

```

1    function plot_opt_contour(topology, ratio, Vin, Iout, Ac, switches, ...
        capacitors, esr, optMethod, plotPoints, plotAxes)
    % plot_opt_contour: Plot optimization contour, including loss-dominant regions
    % Michael Seeman, UC Berkeley
5    %
    % plot_opt_contour(topology, ratio, Vout, Pout, Ac, switches, capacitors
    % [esr, [optMethod, [plotPoints, [plotAxes]]]])
    % topology: The chosen topology to plot contour (a string), or a
    % topology structure or implementation structure
10    % ratio: The step-up ratio of the converter. If a step-down
    % converter is desired, use a fractional ratio (ie. 1/8).
    % Ignored for topology as a structure
    % Vout: Output voltage of converter (in V)
    % Iout: Output current of converter (in A)
15    % Ac: Capacitor area constraint (in m^2). fsw and Ac will be swept
    % switches: a row vector of switch technology structures

```

```

%      capacitors: a row vector of capacitor technology structures
%      esr: the output-referred constant esr of requisite metal (ie, bond
%      wires). Default = 0
20 %      optMethod: specifies constraint on switch optimization (1=area
%      (default), 2=parasitic loss)
%      plotPoints: specifies grid size for contour plot. (default=100)
%      plotAxes: A row vector giving the desired range of the plot, in log
%      input (ie, [6 9 -6 -3] goes from 1MHz-1GHz, 1mm^2-1000mm^2).
25 %
%      Created 4/14/08, Last modified: 4/15/09
%      Copyright 2008-2009, Mike Seeman, UC Berkeley
%      May be freely used and modified but never sold. The original author
%      must be cited in all derivative work.
30
% Fix unspecified parameters:
if nargin < 7, error('plot_opt_contour requires at least seven inputs');
end
if nargin < 10, plotPoints=100;
35     if nargin < 9, optMethod=1;
        if nargin < 8, esr = 0;
        end, end, end

if (ischar(topology)),
40     % topology is a string
    topology = generate_topology(topology, ratio);
    imp = implement_topology(topology, Vin, switches, capacitors, optMethod);
elseif (isfield(topology, 'topology')),
    % topology is an implementation structure
45     imp = topology;
    topology = imp.topology;
    ratio = topology.ratio;
else
    % topology is a topology structure
50     ratio = topology.ratio;
    imp = implement_topology(topology, Vin, switches, capacitors, optMethod);
end

% Constant series resistance, output referred
55 imp.esr = esr;

% Find optimal point for auto axis scaling
[opt_perf, fsw_opt, Asw_opt] = optimize_loss(imp, Vin, Iout, Ac);
opt_perf.Vout
60 if (nargin < 11),
    fsw_min = floor(log10(fsw_opt)-1);
    fsw_max = ceil(log10(fsw_opt)+1);
    Asw_min = floor(log10(Asw_opt)-1);
    Asw_max = ceil(log10(Asw_opt)+1);
65 else
    fsw_min = plotAxes(1);
    fsw_max = plotAxes(2);
    Asw_min = plotAxes(3);
    Asw_max = plotAxes(4);

```

```

70     end

    [fsw, Asw] = meshgrid(logspace(fsw_min,fsw_max,plotPoints),...
        logspace(Asw_min,Asw_max,plotPoints));

75     p = evaluate_loss(imp, Vin, [], Iout, fsw, Asw, Ac);
    [maxeff1, min1] = max(p. efficiency);
    [maxeff, min2] = max(maxeff1');
    min1 = min1(min2);

80     [c,h] = contour(fsw, Asw*1e6, p. efficiency, ...
        [.05 .1 .2 .4 .6 .7 .8 .85 .9 .92 .94 .96 .98 1], 'b-');
    clabel(c,h);
    hold on;
    contour(fsw, Asw*1e6, p. dominant_loss, [1.5 2.5 3.5 4.5], 'k-');
85     loglog(fsw(min1,min2), Asw(min1,min2)*1e6, 'bo');
    hold off;
    xlabel('Switching Frequency [Hz]');
    ylabel('Switch Area [mm^2]');
    title(strcat('I_{OUT} = ', num2str(Iout), 'A, A_{c} = ', num2str(Ac*1e6),...
90         ' mm^2, Eff = ', num2str(maxeff*100,3), ' %'));
    set(gca,'Xscale','log')
    set(gca,'Yscale','log')

```

B.5.7 plot_regulation.m

```

1     function plot_regulation(topologies, Vin, Vout, Iout, Ac, switches, ...
        capacitors, esr, idesign)
    % plot_regulation: Plot efficiency vs. input/output voltage based on fsw-based
    % regulation
5     % Michael Seeman, UC Berkeley
    %
    % plot_regulation2(topologies, Vin, Vout, Pout, Ac, switches, capacitors
    % [noplot, [esr, [optMethod]]])
    %
    % topologies: A matrix of topologies and ratios:
10    %     [{'Series-Parallel'} {1/2};
    %     {'Ladder'} {1/3}]
    %
    % or a column vector of topology or implementation structures
    % Vin: Input voltage of converter (could be a vector)
    % Vout: Output voltage of converter (a vector if Vin is a scalar)
15    % Iout: Matching vector of output currents [A]
    % Ac: Capacitor area constraint (in m^2). fsw will be swept, Asw
    % will be chosen automatically
    % switches: a row vector of switch technology structures
    % capacitors: a row vector of capacitor technology structures
20    % esr: the output-referred constant esr of requisite metal (ie, bond
    % wires). Default = 0
    % idesign: a vector (size = number of topologies) containing the
    % nominal design current for each topology
    %
25    % Created 6/30/08, Last modified: 4/15/09

```

```

% Copyright 2008-2009, Mike Seeman, UC Berkeley
% May be freely used and modified but never sold. The original author
% must be cited in all derivative work.

30 % Fix unspecified parameters:
    if nargin < 7, error('plot_opt_contour needs at least seven input arguments');
    end
    if nargin < 8, esr = 0; end
    optMethod = 1;
35
    type = 0; % 1 = Vout, 2 = Vin swept
    if (size(Vout,2) > 1)
        type = 1;
        indim = size(Vout,2);
40        xval = Vout;
    end
    if (size(Vin,2) > 1)
        if (type == 1),
            error('Cannot sweep both Vin and Vout');
45        end
        type = 2;
        indim = size(Vin,2);
        xval = Vin;
    end
50
    numtops = size(topologies,1); % number of topologies

    EFF = zeros(numtops, indim);
    ASW = [];
55    pkeff = [];
    pkv = [];
    RATIO = [];
    FSW = [];

60    Vin_nom = Vin;

    for t=1:numtops,
        if (iscell(topologies(t,1))),
            % this topology is a string and ratio
65            top = topologies(t,1);
            ratio = cell2mat(topologies(t,2));
            topology = generate_topology(top, ratio);
            if (type == 2), Vin_nom = Vout/ratio; end
            imp = implement_topology(topology, Vin_nom, switches, capacitors, ...
70                optMethod);
        elseif ((size(topologies,2) == 1) && (isfield(topologies(t), 'topology'))),
            % implementation structure
            imp = topologies(t);
            topology = imp.topology;
75            ratio = topology.ratio;
            if (type == 2), Vin_nom = Vout/ratio; end
        elseif (size(topologies,2) == 1),
            topology = topologies(t);

```

```

        ratio = topology.ratio;
80      if (type == 2), Vin_nom = Vout/ratio; end
        imp = implement_topology(topology, Vin_nom, switches, capacitors, ...
            optMethod);
    else
        error('Unknown topology element');
85    end

    % add topology ratio to vector for plot annotation
    RATIO = [RATIO ratio];

90    % calculate nominal design current
    if (nargin < 9)
        if ((type == 1) & (size(Iout,2) == indim))
            Iout_nom = interp1(Vout, Iout, Vin*ratio, 'linear', 'extrap');
        else
95            Iout_nom = max(Iout);
        end
    else
        if (size(idesign,2) > 1), Iout_nom = idesign(t);
        else, Iout_nom = idesign; end
100    end

    % Constant series resistance, output referred
    imp.esr = esr;

105    % Find optimal point for base
    [opt_perf, fsw_opt, Asw_opt] = optimize_loss(imp, Vin_nom, Iout_nom, Ac);
    % ASW(t) = Asw_opt;

    p(t) = evaluate_loss(imp, Vin, Vout, Iout, [], Asw_opt, Ac);
110    EFF(t,:) = p(t).efficiency.*p(t).is_possible;
    % FREQ(t,:) = p(t).fsw;
    [y,i] = max(EFF(t,:));
    pkeff(t) = y;
    pkv(t) = xval(i);
115    end

    [maxeff, mind] = max(EFF);
    % for i=1:size(FREQ,2),
    % fsw(i) = FREQ(mind(i),i);
120    % end

    plot(xval, EFF*100,'b:', xval, maxeff*100, 'b-', pkv, pkeff*100, 'bo');
    if (type == 1),
        xlabel('Output Voltage [V]');
125    elseif (type == 2),
        xlabel('Input Voltage [V]');
    end
    % add labels representing conversion ratios
    for i=1:size(pkv,2),
130        [n, m] = rat(RATIO(i), .001);
        text(pkv(i)*1.01, pkeff(i)*100+1, strcat(num2str(m), ':', num2str(n)));

```



```

end
ylabel('Efficiency [%]');

```

B.5.8 techlib.m

```

1  % Technology Library
   % Copyright 2008-2009, Mike Seeman, UC Berkeley
   % May be freely used and modified but never sold. The original author
   % must be cited in all derivative work.
5
   % ----- Oxide Capacitors
   % 90 nm Oxide Capacitors

   itrs90cap.tech_name = 'ITRS 90nm';
10  itrs90cap.dev_name = 'ITRS 90nm Oxide Capacitor';
   itrs90cap.capacitance = 40^2*1e-15*.7/.09;
   itrs90cap.area = (40e-6*40e-6);           % in m^2
   itrs90cap.bottom_cap = 135.3e-15;         % in F
   itrs90cap.esr = 0;                         % in ohms
15  itrs90cap.rating = 1.2;                   % in V

   % 65 nm Oxide Capacitors

   itrs65cap.tech_name = 'ITRS 65nm';
20  itrs65cap.dev_name = 'ITRS 65nm Oxide Capacitor';
   itrs65cap.capacitance = 40^2*.9e-15*.6/.065;
   itrs65cap.area = (40e-6*40e-6);           % in m^2
   itrs65cap.bottom_cap = 135.3e-15;         % in F
   itrs65cap.esr = 0;                         % in ohms
25  itrs65cap.rating = 1.2;                   % in V

   % 45 nm Oxide Capacitors

   itrs45cap.tech_name = 'ITRS 45nm';
30  itrs45cap.dev_name = 'ITRS 45nm Oxide Capacitor';
   itrs45cap.capacitance = 40^2*.84e-15*.5/.045;
   itrs45cap.area = (40e-6*40e-6);           % in m^2
   itrs45cap.bottom_cap = 135.3e-15;         % in F
   itrs45cap.esr = 0;                         % in ohms
35  itrs45cap.rating = 1.2;                   % in V

   % 32 nm Oxide Capacitors

   itrs32cap.tech_name = 'ITRS 32nm';
40  itrs32cap.dev_name = 'ITRS 32nm Oxide Capacitor';
   itrs32cap.capacitance = 40^2*.8e-15*.45/.032;
   itrs32cap.area = (40e-6*40e-6);           % in m^2
   itrs32cap.bottom_cap = 135.3e-15;         % in F
   itrs32cap.esr = 0;                         % in ohms
45  itrs32cap.rating = 1.2;                   % in V

```

```

% 22 nm Oxide Capacitors

itrs22cap.tech_name = 'ITRS 22nm';
50 itrs22cap.dev_name = 'ITRS 22nm Oxide Capacitor';
itrs22cap.capacitance = 40^2*.58e-15*.4/.022;
itrs22cap.area = (40e-6*40e-6); % in m^2
itrs22cap.bottom_cap = 135.3e-15; % in F
itrs22cap.esr = 0; % in ohms
55 itrs22cap.rating = 1.2; % in V

% 16 nm Oxide Capacitors

itrs16cap.tech_name = 'ITRS 16nm';
60 itrs16cap.dev_name = 'ITRS 16nm Oxide Capacitor';
itrs16cap.capacitance = 40^2*.48e-15*.35/.016;
itrs16cap.area = (40e-6*40e-6); % in m^2
itrs16cap.bottom_cap = 135.3e-15; % in F
itrs16cap.esr = 0; % in ohms
65 itrs16cap.rating = 1.2; % in V

% Filler HV cap

fillercap.tech_name = 'ITRS 16nm';
70 fillercap.dev_name = 'ITRS 16nm Oxide Capacitor';
fillercap.capacitance = 40^2*.48e-15*.35/.016*.01;
fillercap.area = (40e-6*40e-6); % in m^2
fillercap.bottom_cap = 135.3e-15; % in F
fillercap.esr = 0; % in ohms
75 fillercap.rating = 12; % in V

% ----- Switch models

% 90 nm switch
80
itrs90n.tech_name = 'ITRS 90 nm';
itrs90n.dev_name = 'ITRS 90 nm NMOS native transistor';
itrs90n.area = 1e-6 * 90e-9 / .4; % in m^2
itrs90n.conductance = 1.11e-3; % in S
85 itrs90n.gate_rating = 1.25; % in V
itrs90n.drain_rating = 1.25;
itrs90n.gate_cap = 1e-15;
itrs90n.drain_cap = .33*itrs90n.gate_cap;
itrs90n.body_cap = .2*itrs90n.gate_cap;
90

% 65 nm switch

itrs65n.tech_name = 'ITRS 65 nm';
itrs65n.dev_name = 'ITRS 65 nm NMOS native transistor';
95 itrs65n.area = 1e-6 * 65e-9 / .35; % in m^2
itrs65n.conductance = 1.3e-3; % in S
itrs65n.gate_rating = 1.25; % in V
itrs65n.drain_rating = 1.25;
itrs65n.gate_cap = .9e-15;

```

```

100  itrs65n.drain_cap = .33*itrs65n.gate_cap;
    itrs65n.body_cap = .2*itrs65n.gate_cap;

    % 45 nm switch

105  itrs45n.tech_name = 'ITRS 45 nm';
    itrs45n.dev_name = 'ITRS 45 nm NMOS native transistor';
    itrs45n.area = 1e-6 * 45e-9 / .35;      % in m^2
    itrs45n.conductance = 1.51e-3;    % in S
    itrs45n.gate_rating = 1.25;    % in V
110  itrs45n.drain_rating = 1.25;
    itrs45n.gate_cap = .84e-15;
    itrs45n.drain_cap = .33*itrs45n.gate_cap;
    itrs45n.body_cap = .2*itrs45n.gate_cap;

115  % 32 nm switch

    itrs32n.tech_name = 'ITRS 32 nm';
    itrs32n.dev_name = 'ITRS 32 nm NMOS native transistor';
    itrs32n.area = 1e-6 * 32e-9 / .3;      % in m^2
120  itrs32n.conductance = 1.82e-3;    % in S
    itrs32n.gate_rating = 1.25;    % in V
    itrs32n.drain_rating = 1.25;
    itrs32n.gate_cap = .8e-15;
    itrs32n.drain_cap = .33*itrs32n.gate_cap;
125  itrs32n.body_cap = .2*itrs32n.gate_cap;

    % 22 nm switch

    itrs22n.tech_name = 'ITRS 22 nm';
130  itrs22n.dev_name = 'ITRS 22 nm NMOS native transistor';
    itrs22n.area = 1e-6 * 22e-9 / .3;      % in m^2
    itrs22n.conductance = 2.245e-3;    % in S
    itrs22n.gate_rating = 1.25;    % in V
    itrs22n.drain_rating = 1.25;
135  itrs22n.gate_cap = .58e-15;
    itrs22n.drain_cap = .33*itrs22n.gate_cap;
    itrs22n.body_cap = .2*itrs22n.gate_cap;

    % 16 nm switch

140  itrs16n.tech_name = 'ITRS 16 nm';
    itrs16n.dev_name = 'ITRS 16 nm NMOS native transistor';
    itrs16n.area = 1e-6 * 16e-9 / .25;      % in m^2
    itrs16n.conductance = 2.535e-3;    % in S
145  itrs16n.gate_rating = 1.25;    % in V
    itrs16n.drain_rating = 1.25;
    itrs16n.gate_cap = .48e-15;
    itrs16n.drain_cap = .33*itrs16n.gate_cap;
    itrs16n.body_cap = .2*itrs16n.gate_cap;

```

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Index

- analysis code, *see* MATLAB code
- bandgap reference, *see* voltage reference
- boost converter
 - comparison with SC, 67
 - for aerial robotics, 107
- bottom-plate capacitance
 - reducing, 159
- charge multiplier vector, 11, 18, 173
 - for switches, 176
- charge multipliers, 161
 - meaning of sign, 20
- code, *see* MATLAB code
- constraints, optimization
 - capacitor energy, 34
 - die-area, 40
 - parasitic loss, 40
- contour plot, optimization, 44
- converter metric, *see* metric, converter
- current reference, 135
- device cost metric, *see* metric, device
- Dickson topology, 55
- digraph, 165
- doubler topology, 60
- drain charge recovery, 157
- dynamic voltage scaling (DVS), 147
- energy harvesting, 119
- energy per operation, 148
- example
 - charge multipliers, 13, 19
- fast-switching limit (FSL), 5, 18, 21
 - optimized output impedance, 38
- Fibonacci topology, 56
- FLASH; applications, 1
- flyback converter, 110
 - transformer design, 111
- flying capacitor, 3
- FSL, *see* fast-switching limit (FSL)
- fundamental cut set matrix, 167
- fundamental limit
 - FSL Metric, 78
 - SSL Metric, 76
- fundamental loop matrix, 167
- gate drive
 - cascade, 126
 - charge pump, 127
- hybrid SC-boost converter, 112
- hysteretic feedback, 88
 - lower-bound, 90
- inductive load, 26
 - impedance improvement, 29
- interleaved phases, 3, 84
- KCL equation, 171
- KVL equation, 169
- ladder topology, 51
- linear system
 - continuous time, 185
 - discrete time, 188
- link, 166
- load type; SC converter, 11, 25
 - capacitive, 25
 - current source, 26
 - inductive, *see* inductive load
- low-dropout regulator (LDO), 135
- magnetics-based converters, 66
- mass, component, 103
- MATLAB code, 191
 - evaluate_loss, 195, 204
 - generate_topology, 191, 207
 - implement_topology, 192, 212

- optimize_loss, 199, 215
- permute_topologies, 200, 216
- plot_opt_contour, 196, 217
- plot_regulation, 197, 219
- techlib, 222
- metric, converter
 - FSL, 49
 - SSL, 49
- metric, device, 32
 - for capacitors, 32
 - for switches, 33
 - loss-based, 33
- Michael Seeman, *see* awesome
- Micro air vehicle (MAV), 102
- MicroGlider, 103, 116
 - hybrid SC-boost converter, 116
- microprocessor power, 142
 - converter cell size, 150
 - dynamic voltage scaling, 147
 - energy per operation, 148
 - integrated buck converters, 143
 - many-core, 143
 - SC topology, 146
 - technology scaling, 143
- multi-ratio converter, 146
- optimization constraints, *see* constraints,
 - optimization
- optimization contour, 44
- output impedance
 - approximation, 23
 - FSL, 21
 - optimized FSL, 38
 - optimized SSL, 36
 - total, 21, 23
 - two-phase, 24
- phase, 3
- PicoCube, 120
 - system efficiency, 141
- power density
 - components by mass, 104
- prior work, 1, 6, 103
- regulation, 81
 - efficiency improvement, 83
 - hysteretic, 88
 - variable-ratio topologies, 93
- resonant drain, 157
- resonant gate drive, 155
- ripple voltage, output, 84
 - interleaved phases, 85
- RS232; applications, 1
- sample and hold, 137
- SC converter, *see* switched-capacitor converter
- series-parallel topology, 58
- shaker, electromagnetic, 121
- slow-switching limit (SSL), 5, 6, 10
 - eliminating impedance with inductors, 30
 - optimized output impedance, 36
- soft-charging, 26
- SSL, *see* slow-switching limit (SSL)
- switched-capacitor converter, 2
 - load, 11
 - phase, 3
 - stage, 2
 - topology, 2
- symmetrical topologies, 64
- synchronous rectifier, 129
 - efficiency, 139
 - impedance matching, 133
- technology scaling, 143
- Tellegen's Theorem, 13
- topology, 2
 - Dickson, 55
 - doubler, 60
 - Fibonacci, 56
 - ladder, 51
 - series-parallel, 58
 - symmetrical, 64
- tree, 166
- trivial converter, 21
- twig, 166
- two-phase simplifications, 24
- V-A product
 - in a high-ratio boost converter, 109
- voltage reference, 136
 - sample and hold, 137
- well biasing, 159
- wireless sensor node (WSN), 119